University of Mumbai
Examination 2021 under Cluster 06
(Lead College: Vidyavardhini's College of Engg Tech)

Examination for Direct Second Year Students Commencing from 10th April 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III (For DSE Students)

Course Code: ELC303 and Course Name: Digital Logic Circuits

Time: 2 hours Max. Marks: 80

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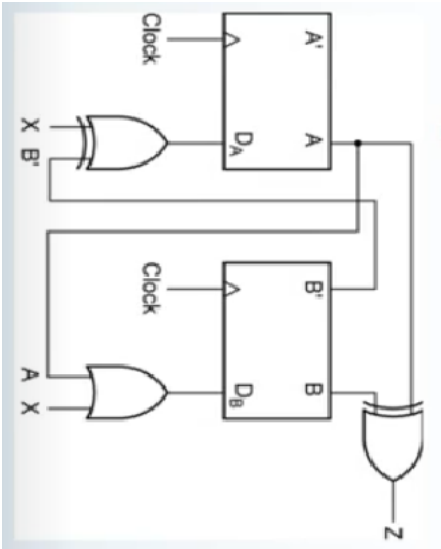
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Convert Decimal $(105)_{10}$ to Binary.
Option A:	$(101001)_2$
Option B:	$(1101001)_2$
Option C:	$(1110101)_2$
Option D:	$(1001011)_2$
2.	In Hamming code this expression will help you to find out number of parity bits.
Option A:	$2^P>=P+M+1$
Option B:	$2^P<=P+M+1$
Option C:	$2^P=P+M-1$
Option D:	$2^P<=P+M-1$
3.	Convert$(125)_8$ octal to binary
Option A:	$(1010101)_2$
Option B:	$(101010)_2$
Option C:	$(1010111)_2$
Option D:	$(11010101)_2$
4.	A multiplexer with 3 select lines is a
Option A:	4:1 multiplexer
Option B:	8:1 multiplexer
Option C:	16:1 multiplexer
Option D:	32:1 multiplexer
5.	IC 74138 is a
Option A:	3:8 line decoder
Option B:	1:8 line decoder
Option C:	4:8 line decoder
Option D:	any lines to 8 line decoder
6.	The IC 74151 can function as a
Option A:	4:1 multiplexer
Option B:	8:1 multiplexer
Option C:	16:1 multiplexer
Option D:	32:1 multiplexer

7.	IC 7485 is a
Option A:	4 bit magnitude comparator
Option B:	4 bit adder
Option C:	4 bit subtractor
Option D:	decoder
8.	Machine whose output depends on present state and external input is :
Option A:	Mealy
Option B:	Sequential asynchronous
Option C:	Asynchronous
Option D:	Moore
9.	Which one of the following is a method of state minimization?
Option A:	Truth table
Option B:	K-map
Option C:	Quine Mcclusky method
Option D:	Implication chart
10.	IC 7492 is a
Option A:	MOD 12 Asynchronous counter
Option B:	MOD 12 Synchronous counter
Option C:	MOD 16 Asynchronous counter
Option D:	MOD 16 Synchronous counter
11.	In IC 74194 when control inputs s1 and s0 are one, it gives _____ operation.
Option A:	Shift right
Option B:	Shift left
Option C:	Hold
Option D:	Load
12.	IC 7490 consist of
Option A:	MOD 6, MOD 2 counter
Option B:	MOD 5, MOD 2 counter
Option C:	MOD 8, MOD 2 counter
Option D:	MOD 5, MOD 3 counter
13.	Condition: IC74163 , CLR=ENP=ENT=1 , LD=0, ABCD=0011, What is the output at pin QD, QC,QB,QA
Option A:	1100
Option B:	0011
Option C:	0101
Option D:	0010
14.	Which of the Logic family dissipate minimum power
Option A:	TTL
Option B:	CMOS
Option C:	DTL
Option D:	ECL

15.	Figure of merit of IC family is
Option A:	Gate propagation delay
Option B:	Gate power Dissipation
Option C:	Speed power product
Option D:	fan out
16.	The number of similar gates which can be driven by a gate is called as
Option A:	Power dissipation
Option B:	Noise margin
Option C:	Fan-out
Option D:	Speed
17.	FPGA stands for
Option A:	Field Programmable Gate Application
Option B:	Field Programmable Gate Array
Option C:	Field Programming Gate Array
Option D:	FET Programmable Gate Array
18.	In procedural assignment _____ data type is used.
Option A:	reg
Option B:	wire
Option C:	wor
Option D:	tri
19.	Operator symbol <<< is a
Option A:	Arithmetic shift left
Option B:	Arithmetic shift right
Option C:	Logical shift left
Option D:	Logical shift right
20.	_____ is a net data type used in Verilog.
Option A:	reg
Option B:	integer
Option C:	real
Option D:	wire

Q2 **(20 Marks)**	
Q2.A	**Solve any Two 5 marks each**
i.	Write short note on Hamming code.
ii.	Compare Melay and Moore Machine.
iii.	Write a program using Verilog HDL for implementing a 4:1 multiplexer using data flow modeling.
Q2.B	**Solve any One 10 marks each**

i.	Implement the function $s = \sum m(1, 2, 4, 7)$ and $c = \sum m(3, 5, 6, 7)$ using a 3:8 decoder IC 74138.
ii.	Explain universal shift register. Design and implement a twisted ring counter using IC 74194.
Q3 (20 Marks)	
Q3.A	**Solve any Two 5 marks each**
i.	Explain with diagram working of IC 7483.
ii.	Write short note on CPLD Architecture.
iii.	Write a program to implement half adder using Verilog HDL.
Q3.B	**Solve any One 10 marks each**
i.	Design MOD-6 counter using IC7490.
ii.	Analyze the given state machine and draw the state diagram. 

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Q1:

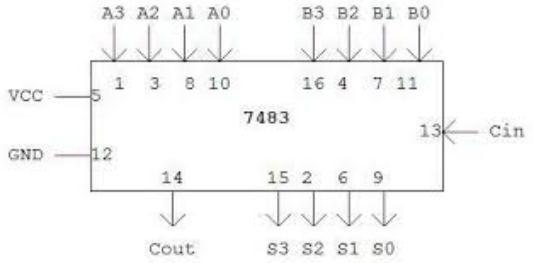
Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	A
Q3.	A
Q4	B
Q5	A
Q6	B
Q7	A
Q8.	A
Q9.	D
Q10.	A
Q11.	D
Q12.	B
Q13.	A
Q14.	B
Q15.	C
Q16.	C
Q17.	B
Q18.	A
Q19.	A
Q20.	D

Important steps and final answer for the questions involving numerical example

Q.2A(ii)IC7483 4 bit Binary Adder

- IC 7483 –Four bit Binary Adder IC
- 4 bit Binary Number A ,4 bits are A3,A2,A1,A0
- 4 bit Binary Number B, 4 bits are B3,B2,B1,B0
- Cin, Cout

Sum we will get at S3,S2,S1,S0

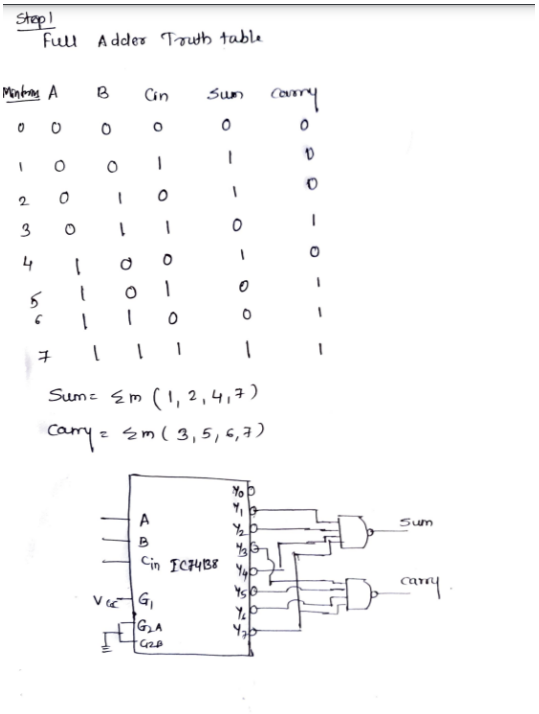


Q.2A(iii)

```
module m41 ( input a,
input b,
input c,
input d,
input s0, s1,
```

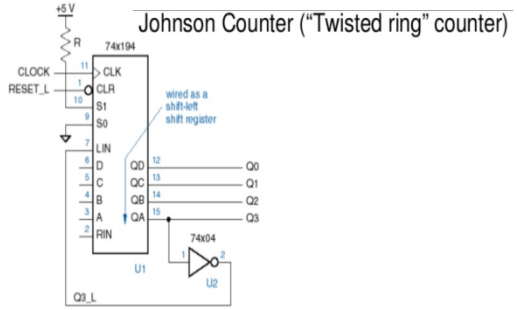
```
output out);
 assign out = s1 ? (s0 ? d
: c) : (s0 ? b : a);


endmodule
```

Q.2B(i)

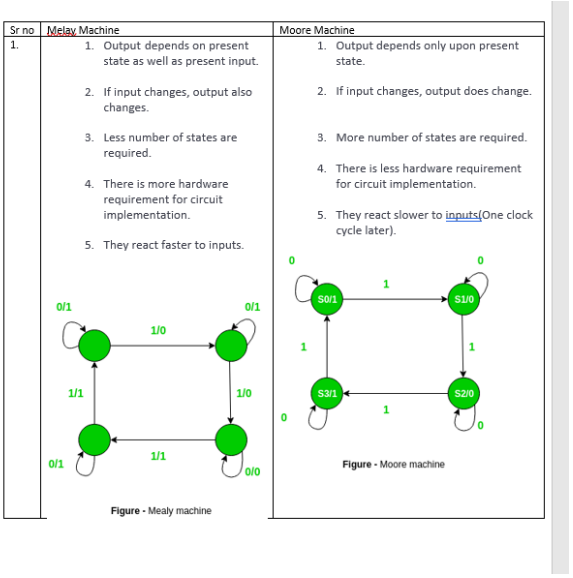


Q.2B(ii)

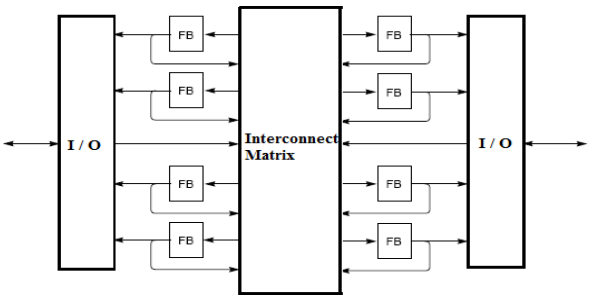
Function	Inputs S1	S0	Next state QA^n	QB^n	QC^n	QD^n
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D



Q.3A(i)



Q.3A(ii) CPLD Architecture:



- The CPLD consists of a number of logic blocks or functional blocks, each of which contains a macrocell and either a PLA or PAL circuit arrangement**.**
- In the diagram eight logic blocks are shown. The building block of the CPLD is the macro-cell, which contains logic implementing disjunctive normal form expressions and more specialized logic operations.

- In the center of the design is a global programmable interconnect.
- This interconnect allows connections to the logic block macrocells and the I/O cell arrays (the digital I/O cells of the CPLD connecting to the pins of the CPLD package).
- The programmable interconnect is usually based on either array-based interconnect or multiplexer-based interconnect

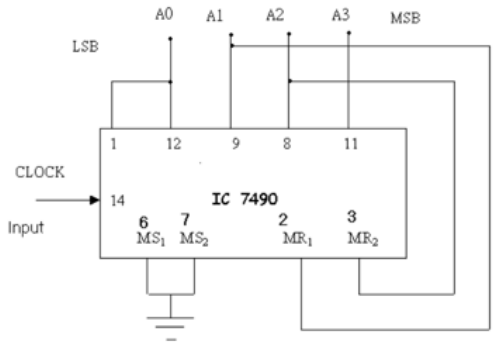
Q.3a(iii)

```
module half_adder (Sum, Carry, A, B);
    input A, B;
    output Carry, Sum;
    //structural description
    xor G1(Sum, A, B);
    and G2(Carry, A, B);
endmodule
```

Q.3b(i)

Asynchronous BCD Decade counter IC 7490

Set pins are active low and reset pins are active high



Q.3b(ii)

Step1:Moore machine

Step2 :Equations

$$A^+ = D_A = X \oplus B'$$
$$B^+ = D_B = A+X$$

Z=A XOR B

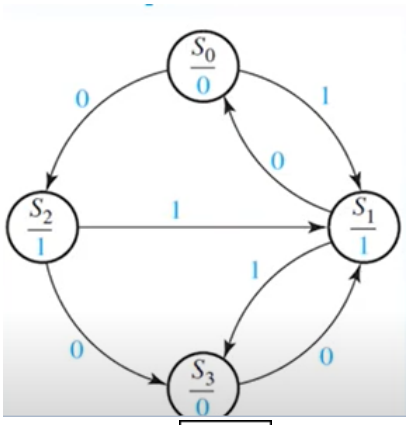
Step3:State transition table

Present State AB	Input X	Next State A^+B^+	Current Output Z
00	0	10	0
	1	01	
01	0	00	1
	1	11	
10	0	11	1
	1	01	
11	0	01	0
	1	11	

Step 4: State assignment

S_0=00, S_1=01,S_2=10,S_3=11

Step 5: State Diagram


S_0
0
S_2
1
S_1
1
S_3
0
0
1
0
1
0
0