University of Mumbai
Examination 2021 under Cluster 06
(Lead College: Vidyavardhini's College of Engg Tech)

Examination for Direct Second Year Students Commencing from 10th April 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III (For DSE Students)

Course Code: ELC302 and Course Name: Electronic Devices and Circuits I

Time: 2 hour   Max. Marks: 80

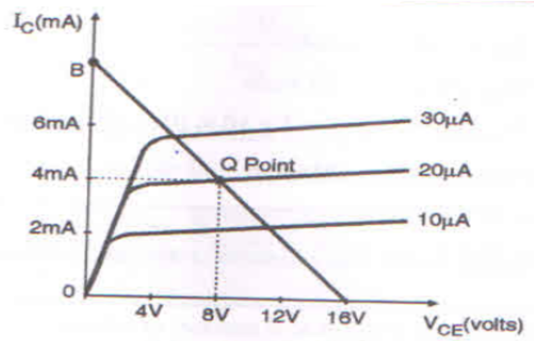
==

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	The *PN* junction allows current flow when
Option A:	*p*-type is more positive than the *n*-type
Option B:	*n*-type is more positive than the *p*-type
Option C:	both the *n*-type and *p*-type have the same positive potential
Option D:	both the *n*-type and *p*-type have the same negative potential
2.	In a PN junction the potential barrier is due to the charges on either side of the junction, these charges are
Option A:	Majority carriers
Option B:	Minority carriers
Option C:	Majority and minority carriers
Option D:	Fixed donor and acceptor ions
3.	Which of the following statement is incorrect?
Option A:	Output of CE amplifier is out of phase with respect to its input
Option B:	CC amplifier is a voltage buffer
Option C:	CB amplifier is a voltage buffer
Option D:	CE amplifier is used as an audio (low frequency) amplifier
4.	The Hybrid-parameters analysis gives correct results for ___________
Option A:	large signals only
Option B:	small signals only
Option C:	both large and small signals
Option D:	Not large nor small signals
5.	How many h-parameters are there for a transistor?
Option A:	Two

Option B:	Three
Option C:	Four
Option D:	Five
6.	The hfe parameter is called ________ in CE arrangement with output short circuited.
Option A:	Voltage Gain
Option B:	Current gain
Option C:	Input impedance
Option D:	Output impedance
7.	How many h-parameters of a transistor are dimensionless?
Option A:	Four
Option B:	Two
Option C:	Three
Option D:	One
8.	In bipolar junction transistor (BJT) the Early effect is due to :-
Option A:	Decrease in width of the emitter due to reverse bias of collector-to-base junction
Option B:	Decrease in width of the base due to reverse bias of collector-to-base junction
Option C:	Decrease in width of collector due to reverse bias of collector-to-base junction
Option D:	Temperature variations resulting in thermally generated minority carriers
9.	In PNP bipolar junction transistor (BJT), stream of current in active region is due to :-
Option A:	Drift of holes
Option B:	Drift of electrons
Option C:	Diffusion of holes
Option D:	Diffusion of electrons
10.	In a bipolar junction transistor (BJT) if $\beta = 100$ & collector current (IC) is 30 mA then what is the value of base current (IB) ?
Option A:	0.3mA
Option B:	0.03 mA
Option C:	30μA
Option D:	0.3μA
11.	In bipolar junction transistor (BJT) which mode of operation is not commonly used in real life applications?
Option A:	The inverse / reverse mode of operation
Option B:	The cut-off mode of operation
Option C:	The saturation mode of operation
Option D:	The forward active / linear mode of operation
12.	The MOSFET is almost ideal as switching device because
Option A:	It has longer life
Option B:	It works progressively
Option C:	It consumes low power
Option D:	It has linear characteristics

13.	MOSFET turn on when
Option A:	VGS>VT
Option B:	VGS<VT
Option C:	VGS=0
Option D:	VDS=VT
14.	The small signal output resistance of r_o of MOSFET is
Option A:	$[\lambda I_{DO}]^{-2}$
Option B:	$[\lambda I_{DO}]^{-1}$
Option C:	$[\lambda I_{DO}]^{-3}$
Option D:	$[\lambda I_{DO}]^{+1}$
15.	Which of the following device has the highest input impedance?
Option A:	JFET
Option B:	MOSFET
Option C:	Crystal Diode
Option D:	BJT
16.	What is the equation of VG for n-channel E-MOSFET in Voltage divider bias configuration?
Option A:	VG = [R2/(R1+R2)]VDS
Option B:	VG = [R1/(R1+R2)]VDD
Option C:	VG = [R1R2/(R1+R2)]VDS
Option D:	VG =[R2/(R1+R2)]VDD
17.	Biasing used in E- MOSFET
Option A:	Fixed bias, self-bias, collector to Base bias, voltage divider bias
Option B:	Fixed bias, collector to Base bias, voltage divider bias
Option C:	Feedback bias ,voltage divider bias
Option D:	Self-bias , collector to Base bias, voltage divider bias
18.	In MOSFET, which terminal is electrically isolated from the entire device structure?
Option A:	Source (S)
Option B:	Drain (D)
Option C:	Gate (G)
Option D:	Bulk or Body or Substrate (SS)
19.	Which is the most suitable biasing circuit for CE Amplifier design?
Option A:	Fixed Bias
Option B:	Fixed bias with R_E
Option C:	Collector to base bias
Option D:	Voltage divider bias
20.	In design of filters, which of these has the lowest value of ripple factor (γ) ?
Option A:	Capacitor (C) Filter
Option B:	Inductor (L) Filter

Option C:	Inductor & Capacitor (L-C) Filter
Option D:	C-L-C or ‘π’ Filter

Q2 **(20 Marks)**	
Q.2 A)	**Solve any two out of three (5 marks each)**
1.	Describe the V-I characteristic of P-N Junction diode with neat labeled diagram.
2.	The DC load line of fixed bias is shown in fig below Determine the required value of VCC, RC and RB for the fixed Bias circuit.  Fig. 1
3.	Explain Bias compensation for BJT(bipolar Junction Transistor).
Q.2 B)	**Solve any one question out of two (10 marks each)**
1	Design single stage CE amplifier for the following specification AV≥100, Vo= 2.5 V f_L=20Hz, stability factor S=10 , use transistor BC147A.hfe=220, hie=2.7KΩ and $V_{CE(SAT)=}$0.25V
2.	For the circuit shown below in Fig. 2, calculate Av, Ri, Ro.

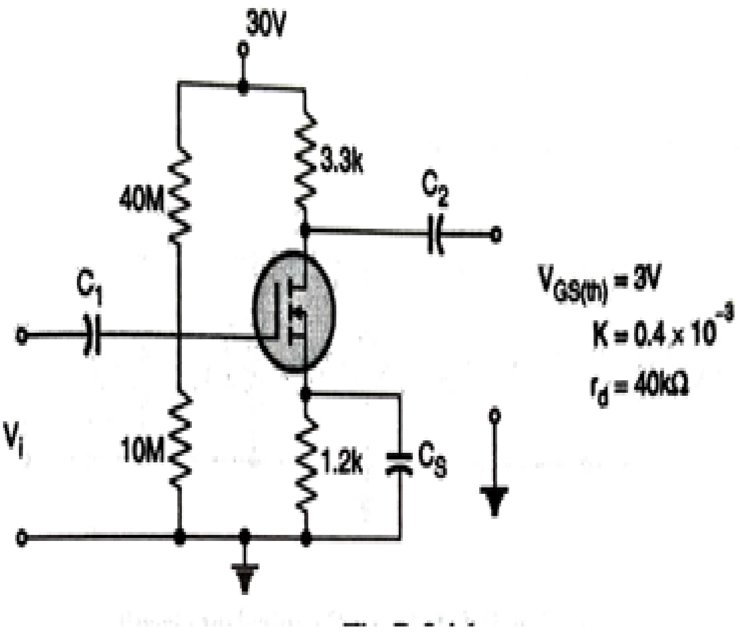
<table>
<tr><td></td><td>


Fig 2.
</td></tr>
</table>

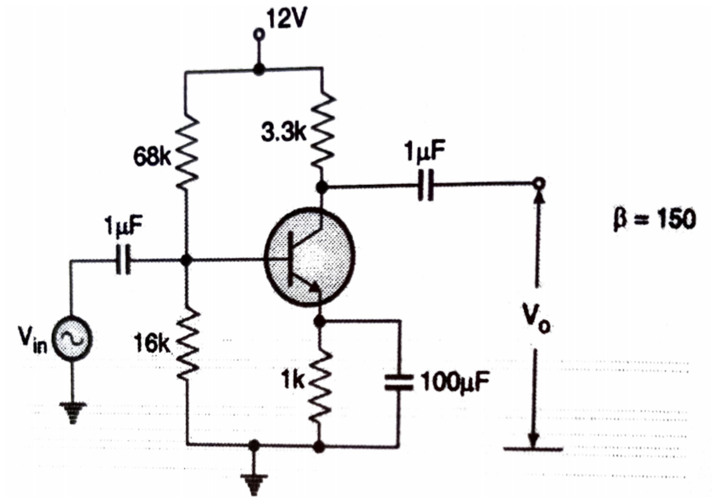
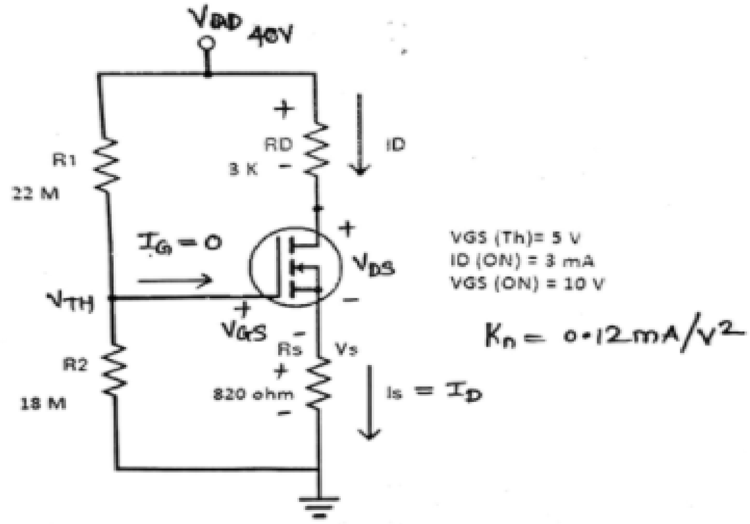
<table>
<tr><td>Q3.
(20 Marks)</td><td>Solve any Two Questions out of Three (10 marks each)</td></tr>
<tr><td>A</td><td>For the given BJT circuit in fig 3.a, find Voltage Gain, Input Resistance and output resistance.


Fig 3.a
</td></tr>
<tr><td>B</td><td>For the voltage divider bias circuit using N-channel E-MOSFET shown in Fig. 3.b, calculate Q – point where Q = [V_{DSQ}, I_{DQ}].</td></tr>
</table>

	 Fig 3.b
C	Design a single stage CE amplifier with FL=10 Hz, Voltage gain AV is 80 output voltage Vo=4.5 V and stability factor S=8. Use BC147A having hfe=220, hie=2.7KΩ and $V_{CE(SAT)=}$0.25V.

University of Mumbai
Examination 2021 under Cluster 06
(Lead College: Vidyavardhini's College of Engg Tech)

Examination for Direct Second Year Students Commencing from 10th April 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III (For DSE Students)

Course Code: ELC302 and Course Name: Electronic Devices and Circuits I

Time: 2 hour Max. Marks: 80

==

Q1:

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	A
Q2.	D
Q3.	C
Q4	B
Q5	C
Q6	B
Q7	B
Q8.	B
Q9.	C
Q10.	A
Q11.	A
Q12.	C
Q13.	A
Q14.	B
Q15.	B
Q16.	D
Q17.	C
Q18.	C
Q19.	D
Q20.	D

Important steps and final answer for the questions involving numerical example

Q2(A)(2):

Q.2 A) 2) For the Fixed Bias circuit

- From the Load Line, we get

$[V_{CC} = 16\,V \quad I_{Cmax} = 8\,mA]$

$$\therefore R_B = \frac{V_{CC} - V_{BE}}{I_{BQ}}$$

$$= \frac{16 - 0.7}{20\,\mu A}$$

$$\boxed{R_B = 765\,k\Omega}$$

$$R_C = \frac{V_{CC} - V_{CE}}{I_{CQ}}$$

$$R_C = \frac{16 - 8}{4\,mA}$$

$$\boxed{R_C = 2\,k\Omega}$$

Q.2(B) (2):-

. DC Analaysis

$V_{GSQ} = V_G - V_S = V_G - I_D R_S$

$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} = \frac{10}{40+10} \times 30$

$V_G = 6\,V \longrightarrow (1)$

$V_{GSQ} = (6 - 1.2 I_{DQ})$.

$I_{DQ} = K[V_{GSQ} - V_T]^2$

$= 0.4[6 - 1.2 I_{DQ} - 3]^2$

$I_{DQ} = 0.4[9 - 7.2 I_{DQ} - 1.44 I_{DQ}^2]$

$1.44 I_{DQ}^2 - 9.7 I_{DQ} + 9 = 0$

$I_{DQ} = 1.11\,mA \longrightarrow (2)$

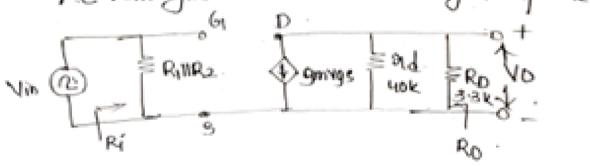
$V_{GSQ} = 6 - (1.2 \times 1.11) = 4.665\,V \rightarrow (3)$

$g_m = 2K(V_{GSQ} - V_T)$

$= 2 \times 0.4 (4.665 - 3)$.

$g_m = 1.33\,mA/V \longrightarrow (4)$.

AC Analaysis $\rightarrow$ Draw Small signal eqⁿ ckt



$R_i = R_1 \| R_2 = 40 \| 10$

$$\boxed{R_i = 8\,M\Omega}$$

$R_O = r_d \| R_D = 40k \| 3.3k$.

$$\boxed{R_O = 3.048\,k\Omega}$$

$A_V = -g_m (r_d \| R_D)$

$= -1.33 (40k \| 3.3k)$

$$\boxed{A_V = -4.054.}$$

Q.3 A). Given ⇒ $\beta = 150$ $V_A = \infty$

DC Analysis.

$V_{th} = \frac{R_2}{R_1+R_2} V_{CC} = \frac{16}{68+16} \times 12 = 2.29V.$

$R_B = R_1 \| R_2 = 12.95 k\Omega.$

$I_{BQ} = \frac{V_{th} - V_{BE}}{R_B + (1+\beta)R_E} = 9.7 \mu A.$

$I_{CQ} = \beta I_{BQ} = 1.47mA.$

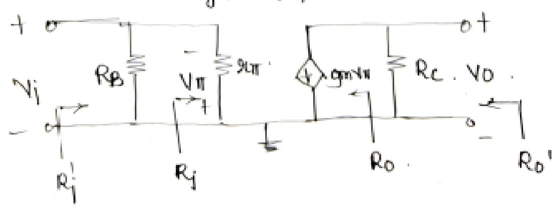
$V_T = 26mV$ $r_\pi = \frac{V_T \beta}{I_{CQ}} = 2.67 k\Omega$

$g_m = \frac{I_{CQ}}{V_T} = 56.15 mA/V.$

$r_o = \frac{V_A}{I_{CQ}} = \infty.$

Small Signal Analysis.

Draw the small signal model



$R_i = r_\pi = 2.67 k\Omega.$

$R_i' = R_B \| R_i = 2.67k \| 12.95k = 2.21 k\Omega.$

$R_o = \infty.$

$R_o' = R_C = 3.3k.$

$A_v = \frac{V_o}{V_i} = \frac{-g_m V_\pi R_C}{V_\pi}$

$= -g_m R_C$

$= -56.15 \times 3.3$

$A_v = -185.3.$

Q.3(B)

Q.3 B) E-MOSFET Voltage divider Biasing

$K_n = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_{GS(TH)}]^2} = \frac{3mA}{[10-5]^2} = 0.12$

$V_{GS} = V_{TH} - I_D R_S = 18 - 0.82 I_D \rightarrow (2)$

$I_D = K_n [V_{GS} - V_{GS(TH)}]^2 \rightarrow (3)$

$I_D = 0.12[18 - 0.82 I_D - 5]^2 \rightarrow (4)$

Hence $I_D = 6.725mA.$ — (5)

$V_{DS} = V_{DD} - I_D(R_D + R_S) = 40 - 6.725[3 + 0.82]$

$V_{DS} = 14.31V$

$Q[V_{DS}, I_D] = [14.31V, 6.725mA].$