University of Mumbai

Examination 2021 under cluster 5 (Lead College: APSIT)

Examinations Commencing from 10th April 2021 to 17th April 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC303** and Course Name: **Digital System Design**

Time: 2 hour Max. Marks: 80

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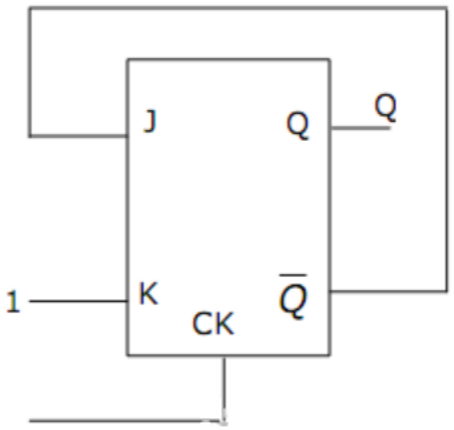
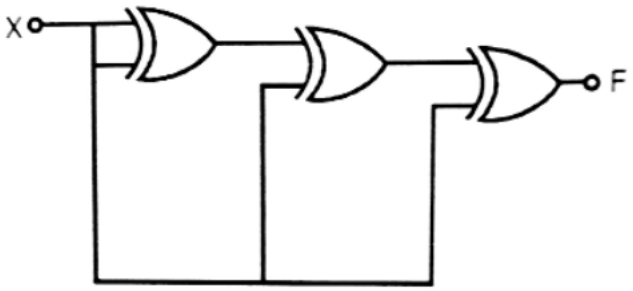
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.**
1.	The decimal equivalent of hex number 1A53 is
Option A:	$(2053)_{10}$
Option B:	$(6739)_{10}$
Option C:	$(2050)_{10}$
Option D:	$(6736)_{10}$
2.	Which one of the following statements best describes the operation of a negative edge triggered D flip flop?
Option A:	The logic level at D input is transferred to Q at the negative edge of the clock
Option B:	The Q output is always identical to the clock input if the D input is high
Option C:	The Q output is always equal to the D input when the clock is positive
Option D:	The Q output is always equal to the D input
3.	In a J K flip flop, we have J =Q' and K=1. Assume the flip flop was initially cleared and then clocked for 6 pulses, the sequence at the output will be 
Option A:	010000
Option B:	011001
Option C:	010010
Option D:	010101
4.	In a positive edge triggered JK flip flop, a low J and low K produces?
Option A:	High state

Option B:	Low state
Option C:	Toggle state
Option D:	No Change State
5.	Decimal 43 in Hexadecimal and BCD number system is respectively
Option A:	B2, 0100 0011
Option B:	2B, 0100 0011
Option C:	2B, 0011 0100
Option D:	B2, 0100 0100
6.	On subtracting (01010)2 from (11110)2 using 1's complement, we get _____
Option A:	01001
Option B:	11010
Option C:	10101
Option D:	10100
7.	The Boolean expression Y= AB+CD is to be realized using only 2 input NAND gates. The minimum number of gates required is
Option A:	2
Option B:	3
Option C:	4
Option D:	5
8.	For the circuit shown below, the output F is given by 
Option A:	F=1
Option B:	F=0
Option C:	F=X
Option D:	F=X'
9.	The output of a logic gate is '1' when all its inputs are at logic '0'. The gate is either
Option A:	a NAND or an EX-OR gate
Option B:	a NOT or an EX-NOR gate
Option C:	an OR or an EX-NOR gate
Option D:	an AND or an EX-OR gate
10.	The canonical sum of product form of the function y(C,D) = C + D is _____
Option A:	CD + DD + C'C

Option B:	CD + CD’ + C’D
Option C:	DC + DC’ + C’D’
Option D:	CD’ + C’D + C’D’
11.	Complement of the expression A’B + CD’ is
Option A:	(A’ + B)(C’ + D)
Option B:	(A + B’)(C’ + D)
Option C:	(A’ + B')(C’ + D)
Option D:	(A’ + B')(C’ + D')
12.	If each successive code differs from its preceding code by a single bit only then this code is called as
Option A:	BCD code
Option B:	Weighted code
Option C:	Gray code
Option D:	Binary code
13.	The bit sequence 0010 is serially entered (right-most bit first) into a 4-bit parallel out shift register that is initially clear. What are the Q outputs after two clock pulses?
Option A:	0000
Option B:	0010
Option C:	1000
Option D:	1111
14.	Which of the following describes the structure of a VHDL code correctly?
Option A:	Library Declaration; Configuration; Entity Declaration; Architecture Declaration
Option B:	Library Declaration; Entity Declaration; Architecture Declaration; Configurations
Option C:	Library Declaration; Entity Declaration; Configuration; Architecture Declaration
Option D:	Library Declaration; Configuration; Architecture Declaration; Entity Declaration
15.	The difference between a PLA and a PAL is
Option A:	the PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
Option B:	the PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
Option C:	the PAL has more possible product terms than the PLA
Option D:	PALs and PLAs are the same thing.
16.	Which of the following cannot be an output of a magnitude comparator
Option A:	A < B
Option B:	A > B
Option C:	A – B
Option D:	A = B
17.	The number of flip-flops required to construct an 8-bit shift register will be
Option A:	32
Option B:	16
Option C:	4
Option D:	8

18.	Which of the following VHDL design units contain the description of the circuit?
Option A:	Configurations
Option B:	Architecture
Option C:	Library
Option D:	Entity
19.	The addition of binary numbers 10011011010 and 010100101 is
Option A:	10101111111
Option B:	1100110110
Option C:	10011010011
Option D:	0111001000
20.	A product term containing all K variables of the function in either complemented or uncomplemented form is called
Option A:	Minterm
Option B:	Maxterm
Option C:	Midterm
Option D:	Least term

Q2.	**Answer the following:**
A	**Solve any Two** **5 marks each**
i.	Convert J-K flip flop to D flip flop.
ii.	Prove that NAND and NOR gates are universal gates.
iii.	Compare PAL with PLA.
B	**Solve any One** **10 marks each**
i.	What is a shift register? Explain working of Serial In Serial Out shift register?
ii.	Minimize the following expression using Quine McClusky technique. $F(A, B, C, D) = \sum m(1,3,7,11,15) + d(0,2,5)$

Q3.	**Answer the following:**
A	**Solve any Two** **5 marks each**
i.	Convert $(365.24)_8$ into decimal, binary and hexadecimal.
ii.	Write VHDL code for the full subtractor.
iii.	For the given minterms, obtain the simplified POS expression $F(A, B, C, D) = \sum m(2,3,5,7,12) + d(6, 13, 14, 15)$
B	**Solve any One** **10 marks each**
i.	With the help of a truth table explain the full adder circuit and implement it using logic gates.
ii.	Design 3 bit binary to gray code converter.

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	A
Q3.	D
Q4.	D
Q5.	B
Q6.	D
Q7.	B
Q8.	B
Q9.	B
Q10.	B
Q11.	B
Q12.	C
Q13.	C
Q14.	B
Q15.	B
Q16.	C
Q17.	D
Q18.	B
Q19.	A
Q20.	A