K. J. Somaiya Institute of Engineering and Information Technology
Sion, Mumbai - 400022
NAAC Accredited Institute with 'A' Grade
NBA Accredited 3 Programs
(Computer Engineering, Electronics & Telecommunication Engineering and Electronics Engineering)
Permanently Affiliated to University of Mumbai

EXAMINATION TIME TABLE (JANUARY 2021)

PROGRAMME - T.E. (Computer) (REV. -2012)(CBSGS)

SEMESTER - V

Days and Dates	Time	Course Code	Paper
Thursday, January 7, 2021	3.30 p.m to 5.30 p.m	CPC501	MICROPROCESSOR
Saturday, January 9, 2021	3.30 p.m to 5.30 p.m	CPC502	OPERATING SYSTEMS
Tuesday, January 12, 2021	3.30 p.m to 5.30 p.m	CPC503	STRUCTURED AND OBJECT ORIENTED ANALYSIS & DESIGN
Thursday, January 14, 2021	3.30 p.m to 5.30 p.m	CPC504	COMPUTER NETWORKS

Important Note: ● **Change if any, in the time table shall be communicated on the college web site.**

PRINCIPAL

Mumbai
20th December 2020

University of Mumbai

Examination 2020 under cluster _4_(Lead College: PCE)

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: **Computer Engineering**

Curriculum Scheme: 2012

Examination: TE Semester V

Course Code: CPC501 and Course Name: Microprocessor

Time: 2 hour Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	The instruction queue of 8086 processor is of
Option A:	8 bytes
Option B:	6 bytes
Option C:	8 bits
Option D:	6 bits
2.	The general purpose register of 8086 comprises of
Option A:	Data segment
Option B:	Code segment
Option C:	Instruction pointer
Option D:	Base register
3.	The signals used for memory segmentation are
Option A:	A0, ˜RD
Option B:	A0, ˜WR
Option C:	˜BHE, ˜RD
Option D:	˜BHE, A0
4.	Addressing modes used in 8086 includes
Option A:	Paging and segmentation
Option B:	Read and write mode
Option C:	Implied and implicit mode
Option D:	Minimum and maximum mode
5.	Executing an assembly program creates _____files
Option A:	.ASM and .EXE
Option B:	.EXE and .OBJ
Option C:	LINK and TD
Option D:	.ASM and .OBJ
6.	PPI is represented by the IC
Option A:	8255
Option B:	8259
Option C:	8257
Option D:	8237

7.	To interface 8 KB of memory the number of address lines required are____
Option A:	A0-A13
Option B:	A0-A12
Option C:	A1-A12
Option D:	A0-A14
8.	In cascading 8259, the maximum number of interrupts that can be connected are__
Option A:	64
Option B:	8
Option C:	16
Option D:	4
9.	MESI model of Pentium represents
Option A:	Modified, Exclusive, Shared, Intercept protocol
Option B:	Modified, Exclusive, Shared, Interval protocol
Option C:	Modified, Exclusive, Shared, Interrupt protocol
Option D:	Modified, Exclusive, Shared, Invalid protocol
10.	Virtual memory of 80386 can be addressed as ___ when used for a single task in protected mode.
Option A:	32 GB
Option B:	64 MB
Option C:	64 TB
Option D:	32 TB
11.	Descriptor table of 80386 consists of
Option A:	segment
Option B:	Access byte
Option C:	Mnemonics
Option D:	Operation code
12.	2 way super scalar architecture indicates there are _____
Option A:	2 pipelines
Option B:	4 pipelines
Option C:	6 pipelines
Option D:	8 pipelines
13.	Pentium has_____size of BTB
Option A:	128 entry
Option B:	64 entry
Option C:	256 entry
Option D:	32 entry
14.	If MN/~MX is low the 8086 operates in_____
Option A:	Protected
Option B:	Minimum
Option C:	Real
Option D:	Maximum

15.	For the selected channel to be disabled in IC 8257, the following condition needs to be satisfied:
Option A:	Auto load is set
Option B:	TC STOP bit is set
Option C:	TC STOP bit is reset
Option D:	Auto load is reset
16.	The mode needed to set the interrupt on terminal count in IC 8253 has to operate in _____.
Option A:	Mode 0
Option B:	Mode 1
Option C:	Mode 2
Option D:	Mode 3
17.	The mode in IC 8255 that uses pins of only port C is_____ mode
Option A:	BSR mode
Option B:	Mode 0
Option C:	Mode 1
Option D:	Mode 2
18.	The instructions starting with MOV or ADD are called as _____
Option A:	Commands
Option B:	Operators
Option C:	Opcode
Option D:	Operand
19.	In Superscalar architecture, _____identifies the instructions that are to be issued concurrently at run time
Option A:	Branch prediction logic
Option B:	Firmware
Option C:	Software
Option D:	Hardware
20.	Three modules IU,FPU and CU are specific to _____
Option A:	Pentium Processor
Option B:	SPARC Processor
Option C:	8086 Processor
Option D:	80386DX Processor

Q2 **(20 Marks Each)**	**Solve any Four out of Six5 marks each** ***Please delete the instruction shown in front of every sub question***
A	Explain the programmer's model of 8086 with a neat diagram.
B	Explain the read cycle timing diagram for minimum mode of operation
C	Define assembler directives and explain any four of them.
D	Write a program to generate a delay of 100 milliseconds using 8086 systems that runs on 10 MHz frequency
E	Write a program to move a byte string which is 16 byte long from location 2000 to 8000 location. Assume the segment it was to be 9000 also determine the physical address for the same
F	Explain ICW1 and ICW 2 of 8259

Q3 **(20 Marks Each)**	**Solve any Four out of Six5 marks each** ***Please delete the instruction shown in front of every sub question***
A	For Interfacing 2- 4k *8 EEPROM and 2- 4k*8 RAMs with 8086 , determine 1. Number of chips required 2. Address map for the same
B	Draw interfacing diagram to connect 2- 8255 in IO mode, 1-8254 in mode 2, 1-8237 in burst mode with 8086
C	Differentiate between real mode, protected mode and virtual mode
D	Explain page address translation mechanism in 80386 with details of PDE and PTE
E	Draw and explain integer pipeline stages of Pentium
F	Explain branch prediction logic of Pentium processor in detail

University of Mumbai

Examination 2020 under cluster _4_(Lead College: PCE)

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Program: **Computer Engineering**

Curriculum Scheme: 2012

Examination: TE Semester V

Course Code: CPC501 and Course Name: Microprocessor

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	D
Q3.	D
Q4	C
Q5	B
Q6	A
Q7	B
Q8.	A
Q9.	D
Q10.	C
Q11.	B
Q12.	A
Q13.	C
Q14.	D
Q15.	B
Q16.	A
Q17.	A
Q18.	C
Q19.	D
Q20.	B

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Examination 2020 under cluster 4 (Lead College: PCE, New Panvel)

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: **Computer Engineering**

Curriculum Scheme: Rev-2012

Examination: TE Semester V

Course Code: CPC502 and Course Name: Operating Systems

Time: 2 hour Max. Marks: 80

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0901_R12_Comp_V_CPC502_AK2

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Multiprogramming is also the ability of an operating system to execute more than one program on a single processor machine. Logical extension of multiprogramming operating system is
Option A:	single programming
Option B:	time sharing
Option C:	multitasking
Option D:	time sharing and multitasking
2.	Kernel mode of operating system is also called
Option A:	supervisor mode
Option B:	user mode
Option C:	system mode
Option D:	burst mode
3.	A process is more than the program code, which is sometimes known as the
Option A:	a text section
Option B:	heap
Option C:	register
Option D:	stack
4.	A process can cause the termination of another process via an appropriate system call. A parent may terminate the execution of one of its children for a variety of reasons. Which of the following is **not an appropriate** reason?
Option A:	The child has exceeded its usage of some of the resources that it has been allocated.
Option B:	The task assigned to the child is no longer required.
Option C:	The parent is exiting, and the operating system does not allow a child to continue if its parent terminates
Option D:	The task assigned to the child is still required, and the child is properly utilising resources allocated to it.
5.	What is dispatching?

Option A:	A job from the job queue is selected and moved to ready queue
Option B:	A process is sent to the processor for execution
Option C:	The Process of saving the status of an interrupted process and loading the status of the scheduled process
Option D:	There is an interrupt to the running process, the process stop and its current status is saved in the PCB
6.	If there is a process with intensive CPU-bursts, that is, longer CPU cycles and a lower number of I/O bursts, then is known as a
Option A:	CPU-bounded process
Option B:	I/O bound process
Option C:	Waiting process
Option D:	Terminating process
7.	a process holds at least one resource and is waiting to acquire a resource held by another process this leads to which possible condition of deadlock?
Option A:	Mutual exclusion
Option B:	Hold and wait
Option C:	No preemption
Option D:	Circular wait
8.	how a deadlock avoidance algorithm confirms that a circular wait condition can never exist ?
Option A:	by examining memory fragmentation
Option B:	by calculating secondary storage limit
Option C:	by PCI bus
Option D:	by examining resource allocation state
9.	If the operating system spends more time in servicing the page faults than actual processing then this situation is called _____.
Option A:	external fragmentation
Option B:	internal fragmentation
Option C:	thrashing
Option D:	compaction
10.	In context of segment to memory frame allocation, Segmentation leads to the problem of _____
Option A:	Internal fragmentation
Option B:	External fragmentation
Option C:	Bounded-buffer
Option D:	Deadlock
11.	In the virtual memory management technique where pages of process are not swapped in all at once but they are swapped in only when the process needs them is called as _____
Option A:	Demand Paging
Option B:	Random access memory
Option C:	Compaction
Option D:	Page table

12.	A …… on free space management has the advantages that it relatively easy to find one or a contiguous group of free blocks.
Option A:	Bit table
Option B:	Chained Free Portion
Option C:	Indexing
Option D:	Free Block List
13.	The _____ might not affect if the data to be accessed on the disk is large and sequential
Option A:	seek time
Option B:	transfer time
Option C:	Rotational latency
Option D:	Disk bandwidth
14.	_____ the processor continually waits for an I/O operation and does not perform any operation
Option A:	DMA
Option B:	programmed IO
Option C:	Interrupt driven IO
Option D:	Kernel IO sub system
15.	Which of the following is not a part of job control facilities?
Option A:	relate a job to the background
Option B:	bring it back to the foreground
Option C:	kill a job
Option D:	create a new job
16.	Each entry of directory file has components namely
Option A:	filename
Option B:	inode number
Option C:	filename and inode number
Option D:	file size
17.	Which command is used to search for pattern matches in a given file?
Option A:	ls
Option B:	ps
Option C:	grep
Option D:	mkdir
18.	if we want to give all file access permissions (i.e read, write and execute) to everyone (i.e ugo) then which chmod command is used?
Option A:	chmod 777
Option B:	chmod 000
Option C:	chmod 421
Option D:	chmod 222
19.	The architecture of Windows is a
Option A:	layered system of module
Option B:	monolithic
Option C:	multi-mode
Option D:	open source

20.	Windows works with the hardware to implement sophisticated strategies for energy efficiency implemented by power managers. The power manager can also put the entire system into a very efficient sleep mode and can even write all the contents of memory to disk and turn off the power to allow the system to go into ____
Option A:	hibernation
Option B:	system restore point
Option C:	file reference
Option D:	power on self test

Q2. **(20 Marks Each)**	
A	**Solve any Two** **5 marks each**
i.	What is an operating system? Explain different functions of operating systems.
ii.	Describe various methods to Recover from the Deadlock
iii.	What is the need of buffering? Discuss single and double buffering
B	**Solve any One** **10 marks each**
i.	Consider the following set of processes with burst time as given Process Burst Time Priority P1 12 3 P2 3 1 P3 5 2 P4 5 4 The processes have assumed to have arrived in the order P1, P2, P3, P4 all at time 0 (zero). Draw Gantt chart for the following scheduling algorithms FCFS, SJF (non-pre-emptive) and priority. Also calculate average turnaround time and average waiting time.
ii.	What is the page? describe how logical address is converted to physical address by using paging technique with the help of appropriate diagram

Q3. **(20 Marks Each)**	
A	**Solve any Two** **5 marks each**
i.	Explain the role of Process Control Block?
ii.	Apply LRU page replacement Algorithms on given page requests (for three frames),calculate number of hits and miss 2,1,3,4,1,3,4,5,2,5,6,1
iii.	How files are arranged in the Unix operating system?
B	**Solve any One** **10 marks each**
i.	What are different allocation methods of file systems?
ii.	What is the deadlock?describe strategies to prevent the deadlock

University of Mumbai

Examination 2020 under cluster 4 (Lead College: PCE, New Panvel)

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Program: **Computer Engineering**

Curriculum Scheme: Rev-2012

Examination: TE Semester V

Course Code: CPC502 and Course Name: Operating Systems

Time: 2 hour Max. Marks: 80

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0901_R12_Comp_V_CPC502_AK2

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	D
Q2.	A
Q3.	A
Q4	D
Q5	B
Q6	A
Q7	B
Q8.	D
Q9.	C
Q10.	B
Q11.	A
Q12.	A
Q13.	C
Q14.	B
Q15.	D
Q16.	C
Q17.	C
Q18.	A
Q19.	A
Q20.	A

Q2. **(20 Marks Each)**	
A	**Solve any Two** **5 marks each**
i.	*Definition of OS-2 marks* *Functions of OS - 3 marks*
ii.	*Deadlock recovery methods like Process Termination(Abort all deadlocked processes,Abort one process at a time until the deadlock cycle is eliminated etc) and Resource Preemption(select victim,rollback etc) - any three valid points with description - 5 marks*
iii.	*need of buffer(availability of memory space i.e. user process must be available) - 1 Marks.* *single buffer(page contain buffer need to lock kernel space buffer solve problem of IO buffering in user space and kernel space) 3marks* *and Double buffering (process not blocked every time read write from device) - 2 marks*
B	**Solve any One** **10 marks each**

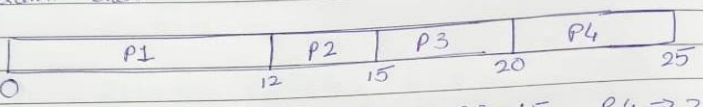
i.

sol^{n} ⇒

Process	Burst time	Priority
P1	12	3
P2	03	1
P3	05	2
P4	05	4

FCFS

Gantt Chart



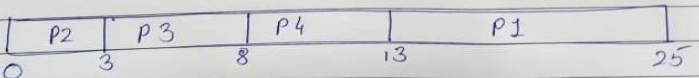
W.T ⇒ P1 ⇒ 0, P2 ⇒ 12, P3 ⇒ 15, P4 ⇒ 20

Avg W.T = (0+12+15+20)/4
= 47/4
= 11.75

T.A.T ⇒ P1 ⇒ 12, P2 ⇒ 15, P3 ⇒ 20, P4 ⇒ 25

Avg T.A.T = (12+15+20+25)/4
= 72/4 = 18

SJF (non-preemptive) Gantt Chart



W.T ⇒ P1 ⇒ 13, P2 ⇒ 0, P3 ⇒ 3, P4 ⇒ 8

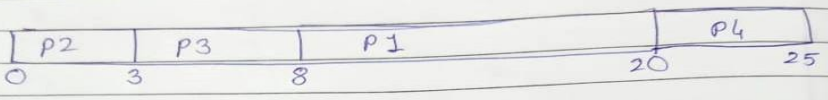
Avg. W.T = (13+0+3+8)/4
= 24/4 = 6

T.A.T ⇒ P1 ⇒ 25, P2 ⇒ 03, P3 ⇒ 08, P4 ⇒ 13

Avg. T.A.T = (25+03+08+13)/4
= 49/4 = 12.25

Priority

Gantt Chart



W.T P1 ⇒ 8, P2 ⇒ 0, P3 ⇒ 3, P4 ⇒ 20

Avg W.T = (8+0+3+20)/4
= 31/4 = 7.75

T.A.T P1 ⇒ 20, P2 ⇒ 03, P4 ⇒ 25, P3 ⇒ 08

Avg T.AT = (20+03+25+08)/4
= 56/4 = 14

	Avg W.T	Avg T.A.T
FCFS	11.75	18
SJF (non preemtive)	06	12.25
Priority	7.75	14

ii.	*definition of page - 2 marks* *paging mechanism with logical to physical address translation by using page table - 8 marks (2 marks for correct diagram of paging hardware + 6 marks for appropriate description)*

Q3. **(20 Marks Each)**	
A	**Solve any Two** **5 marks each**
i.	*Definition of PCB - 1 mark* *Diagram of PCB - 2 marks* *Information contained in PCB to be mentioned - 2 marks*
ii.	
iii.	*I-Node structure diagram -2marks* *file owner identifier and access permission,file type identifier,access time,address of block calculation(direct and indirect) - 3marks*
B	**Solve any One** **10 mark each**
i.	*Contiguous file allocation,Linked file allocation ,Index file allocation(3 marks each) with FAT*
ii.	*definition of deadlock - 2 marks* *deadlock prevention strategy - 8marks (for Mutual exclusion,Hold and wait,No preemption,Circular wait. 2 marks each with proper description)*

University of Mumbai

Examination 2020 under cluster 4 (Lead College: PCE, New Panvel)

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Program: **Computer Engineering**

Curriculum Scheme: **Rev2012**

Examination: **TE Semester V**

Course Code: **CPC503** and Course Name: **Structured and Object Oriented Analysis & Design**

Time: **2hour** Max. Marks: **80**

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Q1.	**Choose the correct option for following questions.** **All questions are compulsory and carry equal marks. (2 marks each)**
1.	Process identification, evaluation with specification & design is part of ----------.
Option A:	requirement engineering
Option B:	feasibility study
Option C:	Business Process Reengineering (BPR)
Option D:	drawing the data flow diagram
2.	---------- are used to capture the exact and detailed requirements of the system to be developed.
Option A:	Feasibility Analysis
Option B:	software testing
Option C:	System architecture
Option D:	Requirement gathering techniques
3.	---------- is a process model used to design, develop and test high quality software.
Option A:	Economic Feasibility
Option B:	Software Development Life Cycle (SDLC)
Option C:	User interface requirements
Option D:	Implementation
4.	The fundamental objective of system analysis is to ----------.
Option A:	study and understand the system
Option B:	understand infrastructure of organisation
Option C:	train the employees
Option D:	sell the product
5.	SRS is abbreviation of the term ----------.
Option A:	Solution for Refining Software
Option B:	Software Requirement Specification
Option C:	Software Resource System
Option D:	System for Reuse of Software
6.	"What, How, When, Who, Where, and Why" are the six viewpoint perspectives of the stakeholders specified in ----------.
Option A:	Zachman Framework
Option B:	Business Process Reengineering

Option C:	System proposal
Option D:	SRS document
7.	Data flow diagrams & E-R diagrams are used in ----------.
Option A:	object-oriented analysis and design
Option B:	Non-structured analysis and design
Option C:	Joint analysis and design
Option D:	structured analysis and design
8.	---------- can be applied to system by providing authorization and authentication to user access.
Option A:	Security controls
Option B:	Database design
Option C:	Use Case Realization
Option D:	Designing of system interfaces
9.	---------- refer to benefits which can't be measured in terms of money.
Option A:	Tangible benefits
Option B:	Direct benefits
Option C:	Indirect benefits
Option D:	Intangible benefits
10.	---------- is measured as cost of usage of printer toner and paper.
Option A:	Variable cost
Option B:	Known cost
Option C:	Fixed cost
Option D:	Direct cost
11.	---------- consists of features of the proposed system, costs, benefits and schedule.
Option A:	Requirement gathering
Option B:	System proposal
Option C:	Waterfall model
Option D:	Process
12.	The time is required before system benefits can overtake the costs of the system is determined in ----------.
Option A:	candidate system
Option B:	net present value
Option C:	return on investment
Option D:	payback analysis
13.	---------- is a graphical representation of the flow of data through an information system.
Option A:	ER diagram
Option B:	Data flow diagram
Option C:	Sequence diagram
Option D:	Activity diagram
14.	In object-oriented analysis and design, ---------- is the main building block.
Option A:	use case

Option B:	Data
Option C:	Object
Option D:	Actor
15.	Inter dependability among modules of a program is called as ----------.
Option A:	Model
Option B:	coupling
Option C:	message
Option D:	interface
16.	Aggregation, association and generalization are the types of relationships shown in ----------.
Option A:	activity diagram
Option B:	state diagram
Option C:	sequence diagram
Option D:	class diagram
17.	---------- are the implementation diagrams in UML.
Option A:	Class & object
Option B:	Component & deployment
Option C:	Sequence & collaboration
Option D:	State & activity
18.	----------is designed such a way that it is expected to provide the user insight of the software.
Option A:	Business process Reengineering
Option B:	Zachman Framework
Option C:	cohesion
Option D:	User interface
19.	---------- deal with all types of flow control in system by using different elements such as fork and join.
Option A:	Activity diagrams
Option B:	Class diagrams
Option C:	Sequence diagrams
Option D:	State diagrams
20.	---------- is anything that interacts with the system, be it a person or another (external) system.
Option A:	Class
Option B:	Method
Option C:	Use-case Actor
Option D:	Message

Q2. **(20 Marks)**	**Solve any Two Questions out of Three.** **(10 marks each)**
A	What is system? Which are the different types of system? Explain the role of system analyst in analyzing, designing and implementation of system.
B	Explain six different types of feasibility study in detail.
C	Explain the purposes of use case diagram. Draw use case diagram for bank ATM example.

Q3. **(20 Marks)**	**Solve any Two Questions out of Three.** **(10 marks each)**
A	Define cohesion and coupling. List and explain the different types of cohesion and coupling in short.
B	Explain the steps to draw Data flow diagram (DFD). Draw the DFD upto level 2 for a payroll system.
C	Explain user interface design in system development. Draw different layouts of graphical user interface (GUI) for online book ordering system.

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Curriculum Scheme: **Rev2012**

Examination: **TE Semester V**

Course Code: **CPC503** and Course Name: **Structured and Object Oriented Analysis & Design**

Time: **2hour** Max. Marks: **80**

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	D
Q3.	B
Q4	A
Q5	B
Q6	A
Q7	D
Q8.	A
Q9.	D
Q10.	A
Q11.	B
Q12.	D
Q13.	B
Q14.	C
Q15.	B
Q16.	D
Q17.	B
Q18.	D
Q19.	A
Q20.	C

Q2. Solve any Two Questions out of Three. **(10 marks each)**

A) What is system? Which are the different types of system? Explain the role of system analyst in analyzing, designing and implementation of system.

Answer: A system is a collection of elements or components that are organized for a common purpose.

Types of System are

1. Physical or Abstract Systems
2. Open or Closed Systems
3. Information Systems

Role of system analyst:

- Identify, understand and plan for organizational and human impacts of planned systems.
- Integrate new technical requirements properly with existing processes and skill sets.
- Interact with internal users and customers to learn and document requirements used to produce business requirements documents.
- Interact with software architect to understand software limitations.
- Help programmers during system development.
- Document requirements or contribute to user manuals.
- Whenever a development process is conducted, the system analyst is responsible for designing components and providing that information to the developer.

B) Explain six different types of feasibility study in detail.

Answer: Six different types of feasibility study are

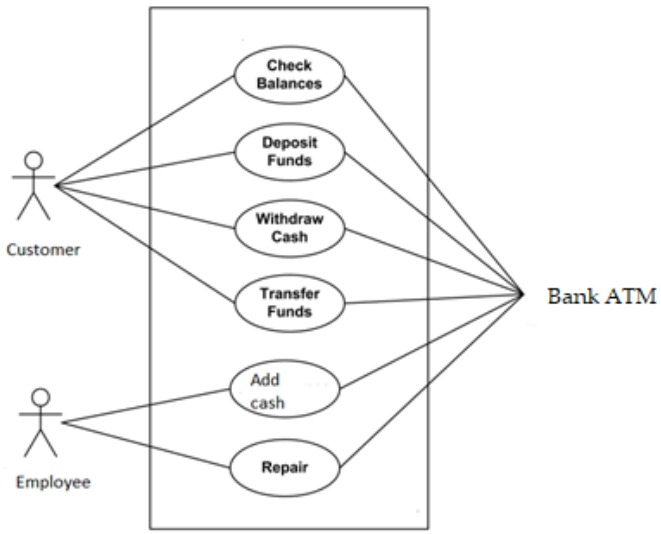
1. **Operational feasibility**
   A measure of how well a solution meets the system requirements.
2. **Cultural (or political) feasibility**
   A measure of how well a solution will be accepted in an organizational climate.
3. **Technical feasibility**
   A measure of the practicality of a technical solution and the availability of technical resources and expertise.
4. **Schedule feasibility**
   A measure of how reasonable the project timetable is.
5. **Economic feasibility**
   A measure of the cost-effectiveness of a project or solution.
6. **Legal feasibility**
   A measure of how well a solution can be implemented within existing legal/contractual obligations.

C) Explain the purposes of use case diagram. Draw use case diagram for bank ATM example.

Answer: The purposes of use case diagram are as follows:

- To capture the dynamic aspect of a system.
- To gather the requirements of a system.
- To identify the external and internal factors influencing the system.
- To show the interaction among the actor and use cases.

Example: Bank ATM Use Case diagram



Q3. Solve any Two Questions out of Three. **(10 marks each)**

A) Define cohesion and coupling. List and explain the different types of cohesion and coupling in short.

Answer:

Cohesion: It is a measure that defines the degree of intra-dependability within elements of a module. The greater the cohesion, the better is the program design.

There are seven types of cohesion, namely

- **Co-incidental cohesion -** It is unplanned and random cohesion, which might be the result of breaking the program into smaller modules for the sake of modularization. Because it is unplanned, it may serve confusion to the programmers and is generally not-accepted.
- **Logical cohesion -** When logically categorized elements are put together into a module, it is called logical cohesion.
- **Temporal Cohesion -** When elements of module are organized such that they are processed at a similar point in time, it is called temporal cohesion.
- **Procedural cohesion -** When elements of module are grouped together, which are executed sequentially in order to perform a task, it is called procedural cohesion.
- **Communicational cohesion -** When elements of module are grouped together, which are executed sequentially and work on same data (information), it is called communicational cohesion.

- **Sequential cohesion -** When elements of module are grouped because the output of one element serves as input to another and so on, it is called sequential cohesion.
- **Functional cohesion -** It is considered to be the highest degree of cohesion, and it is highly expected. Elements of module in functional cohesion are grouped because they all contribute to a single well-defined function. It can also be reused.

Coupling: Coupling is a measure that defines the level of inter-dependability among modules of a program. It tells at what level the modules interfere and interact with each other. The lower the coupling, better the program.

There are five levels of coupling, namely

- **Content coupling -** When a module can directly access or modify or refer to the content of another module, it is called content level coupling.
- **Common coupling-** When multiple modules have read and write access to some global data, it is called common or global coupling.
- **Control coupling-** Two modules are called control-coupled if one of them decides the function of the other module or changes its flow of execution.
- **Stamp coupling-** When multiple modules share common data structure and work on different part of it, it is called stamp coupling.
- **Data coupling-** Data coupling is when two modules interact with each other by means of passing data (as parameter). If a module passes data structure as parameter, then the receiving module should use all its components.

  Ideally, no coupling is considered to be the best.

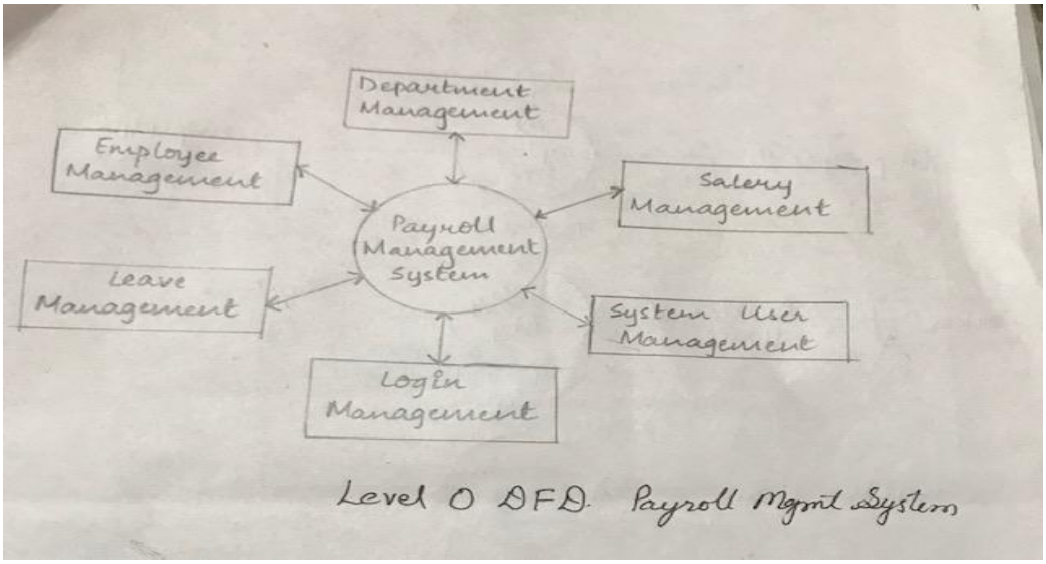
B) Explain the steps to draw Data flow diagram (DFD). Draw the DFD upto level 2 for a payroll system.

Answer: A data flow diagram **(**DFD) shows what kind of information will be input to and output from the system, how the data will advance through the system, and where the data will be stored. It does not show information about process timing or whether processes will operate in sequence or in parallel.

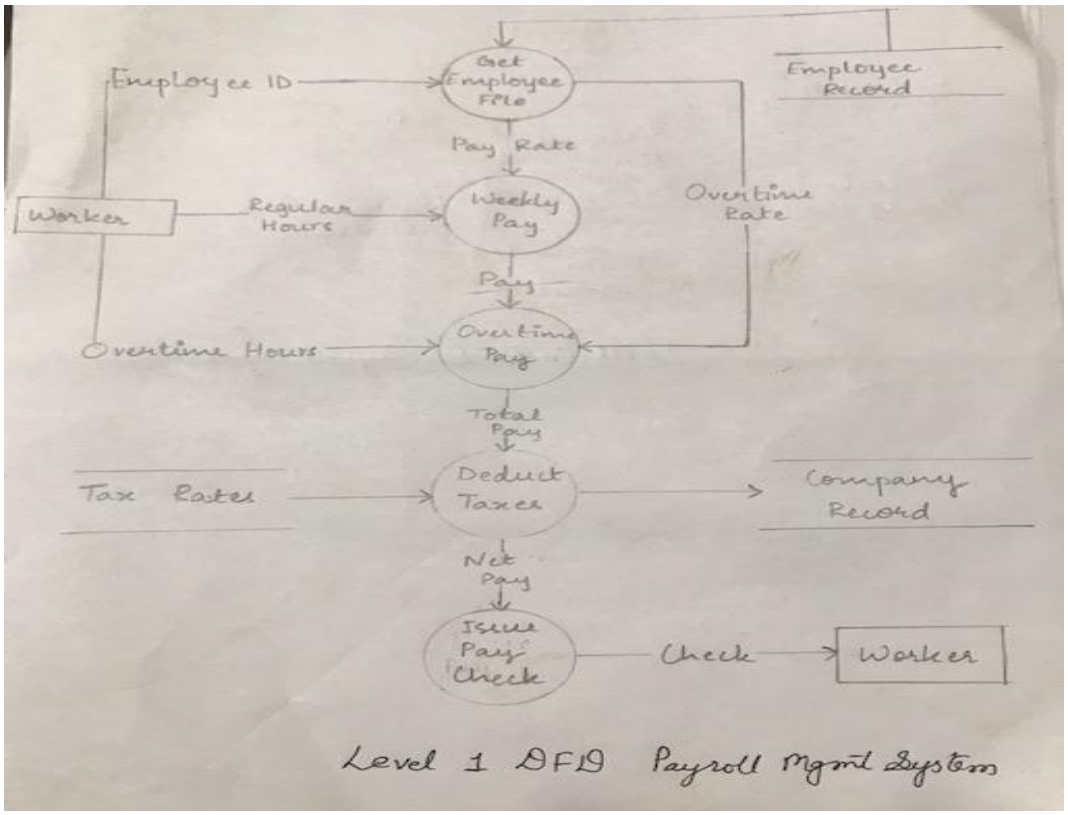
Steps to draw Data Flow Diagram

1. **Draw Context Diagram-**A context diagram is a top level (also known as "Level 0") data flow diagram. It only contains one process node ("Process 0") that generalizes the function of the entire system in relationship to external entities.
2. **Draw different DFD Layers-** Context diagram is followed by various layers of data flow diagrams. A single process node on a high-level diagram can be expanded to show a more detailed data flow diagram. Each of these processes can be broken into further processes until you reach pseudo code.

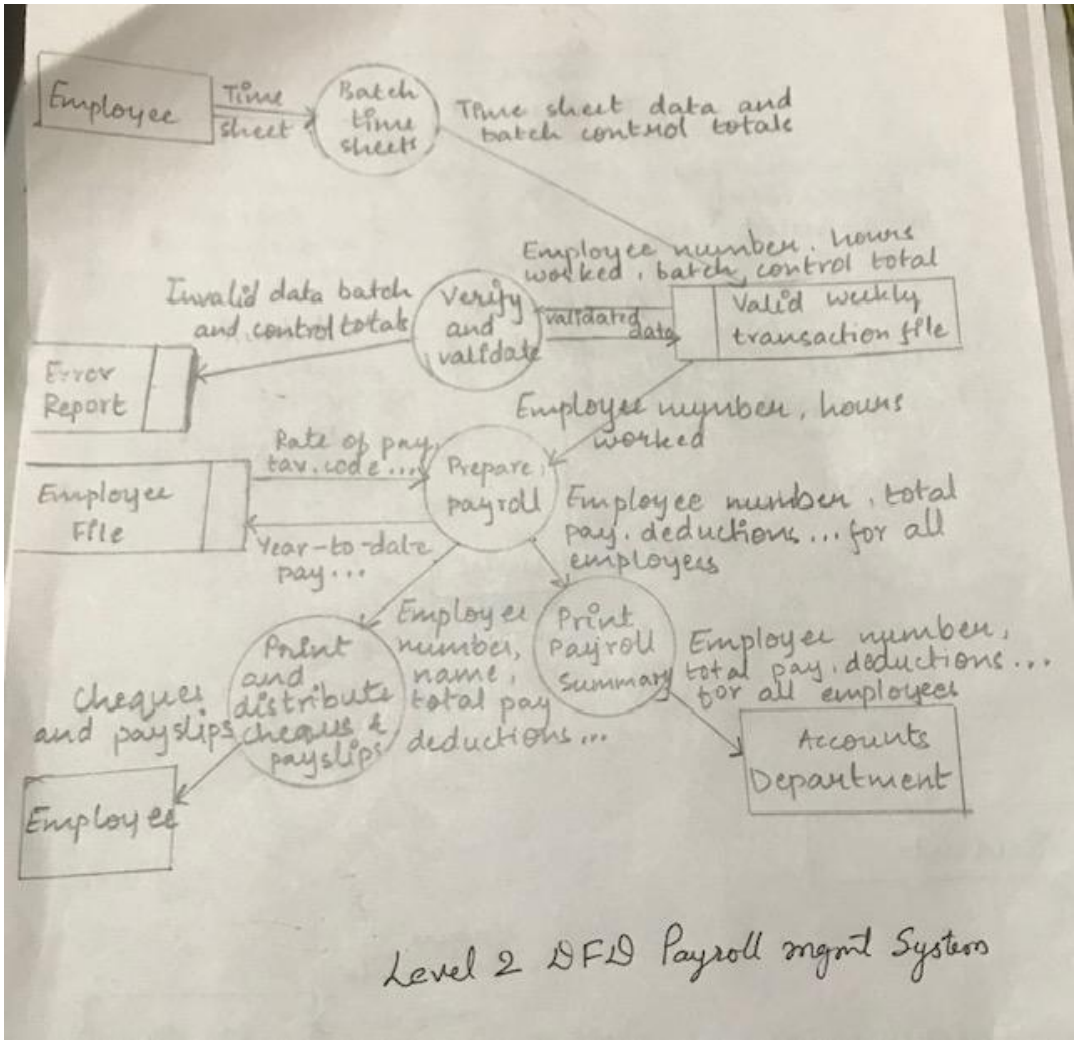
   DFD for a payroll system can be shown as



Level 0 DFD. Payroll Mgmt System



Level 1 DFD Payroll Mgmt System



C) Explain user interface design in system development. Draw different layouts of graphical user interface (GUI) for online book ordering system.

Answer: User interface is the front-end application view to which user interacts in order to use the software. User can manipulate and control the software as well as hardware by means of user interface. Today, user interface is found at almost every place where digital technology exists, right from computers, mobile phones, cars, music players, airplanes, ships etc.

User interface is part of software and is designed such a way that it is expected to provide the user insight of the software. UI provides fundamental platform for human-computer interaction.

UI can be graphical, text-based, audio-video based, depending upon the underlying hardware and software combination. UI can be hardware or software or a combination of both.

User interface must be attractive, simple to use, responsive in short time, clear to understand, consistent on all interfacing screens.

Diagrams are provided for reference only; students may have different views and representations.

University of Mumbai

Examination 2020 under cluster 4 (Lead College: PCE, New Panvel)

Examinations Commencing from 23rd December 2020 to 6th January 2021 and from 7th January 2021 to 20th January 2021

Program: T.E. (Computer) (REV – 2012) (CBSGS)

Curriculum Scheme: 2012

Examination: TE/Semester/V

Course Code: CPC504 and Course Name: Computer Network

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	ARP request is _____ message
Option A:	Broadcast
Option B:	Multicast
Option C:	Unicast
Option D:	Anycast
2.	Routing is the function of which layer?
Option A:	Physical Layer
Option B:	Application Layer
Option C:	Transport Layer
Option D:	Network Layer
3.	Physical layer is responsible for
Option A:	Keeping track of which link connects to which device
Option B:	Allocate network bandwidth to different processes accessing the network
Option C:	Transferring bits from one end to other
Option D:	All of the above
4.	If the bandwidth of the channel is 5 Kbps, how long does it take to send a frame of 100,000 bits out of this device?
Option A:	2 sec
Option B:	20000 sec
Option C:	2000 sec
Option D:	20 sec
5.	Unstuff the following frame payload in which E is escape byte, F is flag byte and D is data byte other than escape or a flag character. E E D E F D D E F E E D D D
Option A:	EEDFDDFEDDD
Option B:	EDFDDFEDDD
Option C:	EDFDDEFEEDDD
Option D:	EDEFDDEFEEDDD
6.	In Adaptive Routing Algorithms
Option A:	Routing decisions are computed in advance, off-line and downloaded
Option B:	Changes routing decisions to reflect changes in the topology, traffic

Option C:	Routing decisions are independent of Topology
Option D:	Traffic parameter is not considered while making decision
7.	Every incoming packet is sent out on every outgoing line except it arrived on is _____
Option A:	Forwarding
Option B:	Multicasting
Option C:	Flooding
Option D:	Unicasting
8.	In classless addressing mask can take any value from
Option A:	0 - 32
Option B:	0 - 255
Option C:	0 – 31
Option D:	0 – 25
9.	Find the error if any in the given IPv4 192.48.12.284
Option A:	Each number can be less than or equal to 255
Option B:	There can be no more than 4 bytes
Option C:	There must be no leading zeros
Option D:	Address must be in binary
10.	SNMP uses the services of UDP on two well-known ports, _____ and _____
Option A:	161; 162
Option B:	160; 161
Option C:	160; 162
Option D:	21, 23
11.	An SNMP agent can send _____ messages.
Option A:	Response
Option B:	GetRequest
Option C:	SetRequest
Option D:	Generate
12.	We can compare the task of network management to the task of writing a program. Both tasks need rules. In network management this is handled by _____.
Option A:	SMNP
Option B:	MIB
Option C:	SMI
Option D:	SMTP
13.	Supernetting is performed on
Option A:	Class E network
Option B:	Class B network
Option C:	Class A network
Option D:	Class C network
14.	Which of the services given below are not provided by network layer?
Option A:	to provide end to end communication between source and destination

Option B:	to provide flow control and error control
Option C:	to route packets via routers
Option D:	to deal with congestion in the network
15.	Which of the following IP address belongs to class B address
Option A:	01111110.11110000.10101000.00110011
Option B:	10000001.11000000.10000000.00000001
Option C:	11000000.00001111.11110000.10101010
Option D:	11100000.01010101.00000001.10000000
16.	A block of addresses is granted to a small organization. We know that one of the addresses is 210.190.37.139/26. What is the first address in the block?
Option A:	210.190.37.0
Option B:	210.190.37.129
Option C:	210.190.37.128
Option D:	210.190.37.139
17.	In Adaptive Routing Algorithms
Option A:	Routing decisions are computed in advance, off-line and downloaded
Option B:	Changes routing decisions to reflect changes in the topology, traffic
Option C:	Routing decisions are independent of Topology
Option D:	Traffic parameter is not considered while making decision
18.	Count to infinity problem is associated with
Option A:	Distance Vector Routing
Option B:	Link state routing
Option C:	Dijkstra's algorithm
Option D:	Flooding
19.	Data Link Layer performs
Option A:	Addressing
Option B:	Routing
Option C:	Framing
Option D:	Session formation
20.	Choke packet is _____
Option A:	closed loop congestion control
Option B:	open loop congestion control
Option C:	Flow control mechanism
Option D:	Error control mechanism

Q2 **(20 Marks)**	**Solve any Two Questions out of Three 10 marks each**
A	For a network with one of the IP Address 192.168.4.77 Find 1. Class 2. Subnet Mask 3. Network Address 4. First available host

	5. Broadcast Address 6. Last Available IP address
B	Draw and explain TCP/IP reference model with OSI Reference Model
C	Message is represented by $M(x) = x^5+x^4+x$ and generating polynomial $G(x) = x^3+x^2+1$. Generate 3 bit CRC and show error correction method.

Q3 **(20 Marks)**	
A	**Solve any Two 5 marks each**
i.	Explain with example IPv4 address classification
ii.	Explain Bluetooth architecture with the help of diagram
iii.	A 7-bit Hamming Code is received as 1011011.Assuming the even parity state whether received codeword is correct or wrong? If wrong, locate the bit in error.
B	**Solve any One** **10 marks each**
i.	What are congestion prevention policies? Explain congestion control in circuit switching.
ii.	Design a network for the customer who has received 200.1.2.0 IP from ISP and wish to divide network into 4 subnets

University of Mumbai

Examination 2020 under cluster 4 (Lead College: PCE, New Panvel)

Program: T.E. (Computer) (REV – 2012) (CBSGS)

Curriculum Scheme: Rev2012

Examination: TE/Semester/V

Course Code: CPC504 and Course Name: Computer Network

Time: 2 hour Max. Marks: 80

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	A
Q2.	D
Q3.	C
Q4	D
Q5	B
Q6	B
Q7	C
Q8.	A
Q9.	A
Q10.	A
Q11.	A
Q12.	C
Q13.	D
Q14.	B
Q15.	B
Q16.	C
Q17.	B
Q18.	A
Q19.	C
Q20.	A

Q.2 A) For a network with one of the IP Address 192.168.4.77
Find

1. Class 1M

2. Subnet Mask 2M

3. Network Address 2M

4. First available host 2M

5. Broadcast Address 2M

6. Last Available IP address 1M

Q.2 B) Draw and explain TCP/IP reference model with OSI Reference Model

Diagram – 3 M

OSI Model Diagram 3M

Comparison 4M

Q.2 C) Message is represented by $M(x) = x^5+x^4+x$ and generating polynomial $G(x) = x^3+x^2+1$. Generate 3 bit CRC and show error correction method.

Bit representation of message and polynomial 1M

Modulo 2 division 5M

Error Detection method 4M

Q. 3 A) i) Explain with example IPv4 address classification

Classes with rage – 3M

Example of each 2M

ii) Explain Bluetooth architecture with the help of diagram

Diagram 3M

Explanation 2M

iii) A 7-bit Hamming Code is received as 1011011.Assuming the even parity state whether received codeword is correct or wrong? If wrong, locate the bit in error.

Identify parity bits – 3M

Calculating Error bit – 2M

Q. 3 B)i) What are congestion prevention policies? Explain congestion control in circuit switching.

Prevention policies – 5M

Congestion control in circuit switching 5M

ii) Design a network for the customer who has received 200.1.2.0 IP from ISP and wish to divide network into 4 subnets

2 marks for each subnet address calculations