University of Mumbai
Examination 2020 under cluster __(Lead College: _____)
Examinations Commencing from 15ʰ June to 26ᵗʰ June 2021
Program: Computer Engineering
Curriculum Scheme: Rev2019
Examination: SE   Semester III
Course Code: **CSC304** and Course Name: **Digital Logic and Computer Architecture**

Time: 2 hour   Max. Marks: 80

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Q1. 40 marks	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks (2marks each)
1.	Convert hexadecimal number (8A9.B4) to binary equivalent.
Option A:	$(100010101001.110101)_2$
Option B:	$(100010101011.101101)_2$
Option C:	$(100010101001.101101)_2$
Option D:	$(100010101001.101011)_2$
2.	Write equivalent binary number for 10101010 gray code
Option A:	11001100
Option B:	10001100
Option C:	11000100
Option D:	11001110
3.	Which of the following the correct expression for two input NOR Gate
Option A:	$A + B$
Option B:	$A . B$
Option C:	$\overline{A} + \overline{B}$
Option D:	$\overline{A + B}$
4.	Program Counter Holds
Option A:	The Instruction
Option B:	The Data
Option C:	Address of the Current Instruction which is executed
Option D:	Address of the Next Instruction to be fetched
5.	Perform binary subtraction using 2's complement representation. 23 - 48 (use 8 bit representation)
Option A:	10001110
Option B:	11110111
Option C:	11100111
Option D:	11001001
6.	Write number (15.5)10 in IEEE754 format
Option A:	41766666H
Option B:	C170000H

Option C:	41780006H
Option D:	41780000H
7.	In Booths Algorithm in one of the step the A=0110 Q=1100 Q_{-1}=0 and count is not zero what it will be the result of Arithmetic Right shift A,Q, Q_{-1}
Option A:	001101100
Option B:	001101101
Option C:	001101110
Option D:	111101100
8.	Perform hexadecimal addition 2F8 + 5A3
Option A:	79B
Option B:	9AB
Option C:	96B
Option D:	89B
9.	Choose correct equation of carry of full adder
Option A:	A OR B AND C_{in}(A XOR B)
Option B:	A AND B OR C_{in}(A XOR B)
Option C:	A AND B AND C_{in}
Option D:	A OR B OR C_{in}
10.	Which method of combination circuit implementation is widely adopted with maximum output functions and minimum requirement of ICs?
Option A:	Multiplexer Method
Option B:	Decoder Method
Option C:	Encoder Method
Option D:	Full Adder
11.	The addressing mode used in an instruction of the form ADD AX , 07h is _____ addressing mode
Option A:	Direct
Option B:	Indirect
Option C:	Immediate
Option D:	Register
12.	State table method is the method for designing
Option A:	Microprogram Control unit
Option B:	Hardwired Control Unit
Option C:	Memory Unit
Option D:	I/O devices
13.	Basic task for control unit is
Option A:	to perform logical operations
Option B:	to perform execution
Option C:	to initiate the resources
Option D:	to decode instructions and generate control signal
14.	Which is not true about Register memory
Option A:	fastest possible access

Option B:	only hundreds of bytes in size
Option C:	Large in Capacity
Option D:	Part of the processor
15.	Cache memory is implemented using
Option A:	Dynamic RAM
Option B:	Static RAM
Option C:	EPROM
Option D:	PROM
16.	Match the memory type with respective erasing mechanism used

Memory Type	Erasing Mechanism
1- ROM & PROM	a- Electrically, Byte-level
2-EPROM	b- Electrically, Block-level
3- EEPROM	c- UV light, Chip Level
4- Flash Memory	d- Not Possible

Option A:	1 - c, 2 - d, 3 - b, 4 – a
Option B:	1 - d, 2 - a, 3 - c, 4 – b
Option C:	1 - d, 2 - b, 3 - a, 4 – c
Option D:	1 - d, 2 - c, 3 - a, 4 – b
17.	In a Pipelined Processing System The Instruction $A \leftarrow 3 + A$ $B \leftarrow 4 \times A$ Leads _____ Hazard
Option A:	Resource Hazard
Option B:	Structural Hazard
Option C:	Data Hazard
Option D:	Branch Hazard
18.	Which is not true about Instruction Pipelining
Option A:	It will improve system performance in terms of throughput.
Option B:	Pipeline rate limited by slowest pipeline stage
Option C:	Unbalanced lengths of pipe stages reduces speedup
Option D:	Pipelining will not be affected by branching instruction.
19.	Flynn's taxonomy classifies computer architectures based on
Option A:	the number of instructions that can be executed
Option B:	how they operate on data.
Option C:	the number of instructions that can be executed and how they operate on data.
Option D:	None of the Above
20.	We can expand the processor bus connection by using
Option A:	SCSI bus
Option B:	PCI bus
Option C:	Controllers
Option D:	Multiple bus

Q2. (20 Marks)	Solve any Four out of Six (5 marks each)
A	Differentiate between Computer Organization and Architecture with a example
B	Describe the detailed Von-Neumann Model with a neat block diagram
C	Explain any five addressing Modes with examples
D	Write Short Note on SR Flip Flop
E	Explain Hardwired control unit design method (state table method)
F	Differentiate between Hardwired control unit and Micro programmed control unit

Q3. (20 Marks)	Solve any two 10 marks each
A	Consider a Cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 128 bytes. Draw the Associative Mapping and Calculate the TAG and WORD size.
B	Draw the flow chart of Booths algorithm for signed multiplication and Perform -7 x -3 using booths algorithm
C	Write short note on Flynn's classification

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	A
Q3.	D
Q4	D
Q5	C
Q6	D
Q7	A
Q8.	D
Q9.	B
Q10.	B
Q11.	C
Q12.	B
Q13.	D
Q14.	C
Q15.	B
Q16.	D
Q17.	C
Q18.	D
Q19.	C
Q20.	B

Q2:

A. For difference 3 marks and example 2 marks

B. Von-Neumann Model block diagram 2 marks and explanation 3 marks

C. For every addressing with block representation or explanation and example allot 1 marks

D. SR Flip Flop diagram 1 mark truth table 1 mark operation 2 mark and draw back 1 mark

E. Explanation of hardwired control unit and state table method 4 marks block diagram 1 mark

F. For every difference allot 1 marks

Q3.

B. Flow chart and explanation 4 marks for numerical 6 marks.

C. Introduction to parallel processing and Flynn's classification 2 marks & explanation to each classification with block diagram and example 8 marks(2 marks for each type)