University of Mumbai
Examination June 2021
Examinations Commencing from 15th June 2021 to 26th June 2021
Program: **Electronics and Telecommunication**

Curriculum Scheme: Rev2019
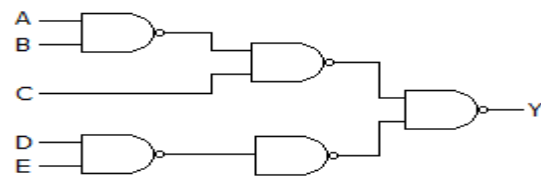
Examination: SE   Semester III

Course Code: ECC303 and Course Name: Digital System Design

Time: 2 Hour   Max. Marks: 80

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Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	A full adder can be made out of …………
Option A:	two half adders
Option B:	two half adders and a OR gate
Option C:	two half adders and a NOT gate
Option D:	three half adders
2.	The circuit of the given figure realizes the function …………
Option A:	$Y = (\overline{A} + \overline{B}) C + \overline{DE}$
Option B:	$Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$
Option C:	$AB + C + DE$
Option D:	$AB + C(D + E)$
3.	What is the hex equivalent of 916, a 4-bit binary number?
Option A:	11112
Option B:	10012
Option C:	01102
Option D:	11002
4.	Which of the following logic families dissipates minimum power ?
Option A:	CMOS
Option B:	ECL
Option C:	TTL
Option D:	DTL
5.	The counter in the given figure is ………….

Option A:	Mod 3
Option B:	Mod 6
Option C:	Mod 8
Option D:	Mod 7
6.	TTL inputs are the emitters of a
Option A:	Transistor-transistor logic
Option B:	Multiple-emitter transistor
Option C:	Resistor-transistor logic
Option D:	Diode-transistor logic
7.	In case of XOR/XNOR simplification, it is required to look for the following:
Option A:	Both Diagonal and Straight Adjacencies
Option B:	Only Offset Adjacencies
Option C:	Both Offset and Straight Adjacencies
Option D:	Both Diagonal and Offset Adjacencies
8.	On addition of 28 and 18 using 2's complement, we get
Option A:	00101110
Option B:	0101110
Option C:	00101111
Option D:	1001111
9.	One example of the use of an S-R flip-flop is as _____
Option A:	Transition pulse generator
Option B:	Racer
Option C:	Switch debouncer
Option D:	Astable oscillator
10.	If enable input is high then the multiplexer is
Option A:	Enable
Option B:	Disable
Option C:	Saturation
Option D:	High Impedance
11.	In D flip-flop, if clock input is LOW, the D input
Option A:	Has no effect
Option B:	Goes high
Option C:	Goes low
Option D:	Has effect
12.	Why is a demultiplexer called a data distributor?

Option A:	The input will be distributed to one of the outputs
Option B:	One of the inputs will be selected for the output
Option C:	The output will be distributed to one of the inputs
Option D:	Single input gives single output
13.	The difference between a PAL & a PLA is
Option A:	PALs and PLAs are the same thing
Option B:	The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane
Option C:	The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane
Option D:	The PAL has more possible product terms than the PLA
14.	PROMs are available in
Option A:	Bipolar and MOSFET technologies
Option B:	MOSFET and FET technologies
Option C:	FET and bipolar technologies
Option D:	MOS and bipolar technologies
15.	The use of VHDL can be done in ways.
Option A:	2
Option B:	3
Option C:	4
Option D:	5
16.	What is the preset condition for a ring shift counter?
Option A:	All FFs set to 1
Option B:	All FFs cleared to 0
Option C:	A single 0, the rest 1
Option D:	A single 1, the rest 0
17.	In a positive edge triggered JK flip flop, a low J and low K produces?
Option A:	High state
Option B:	Low state
Option C:	Toggle state
Option D:	No Change State
18.	Which is the major functioning responsibility of the multiplexing combinational circuit?
Option A:	Decoding the binary information
Option B:	Generation of all minterms in an output function with OR-gate
Option C:	Generation of selected path between multiple sources and a single destination
Option D:	Encoding of binary information
19.	The octal number (651.124)8 is equivalent to
Option A:	(1A9.2A)16
Option B:	(1B0.10)16
Option C:	(1A8.A3)16
Option D:	(1B0.B0)16

20.	The addition of +19 and +43 results as _____ in 2's complement system.
Option A:	11001010
Option B:	101011010
Option C:	00101010
Option D:	0111110

subjective/descriptive questions

Option 1

Q2 (20 Marks Each)	Solve any Four out of Six 5 marks each
A	Compare TTL and CMOS Logic Families.
B	Design full adder using 3:8 decoder.
C	Convert (532.125) base 8, into decimal, binary and hexadecimal.
D	VHDL Code for full subtractor.
E	Convert SR Flip Flop to JK Flip Flop.
F	Compare SRAM with DRAM .

Option 2

Q3. (20 Marks Each)	Solve any Two Questions out of Three 10 marks each
A	Design 3 bit binary to gray converter.
B	Minimize the following expression using Quine Mc-cluskey technique. $F(A,B,C,D)=\sum M(0,1,2,3,5,7,9,11)$
C	Design Synchronous counter using D-type flip flops for getting the following sequence 0-2-4-6-0.take care of lockout condition.

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	A
Q3.	B
Q4	A
Q5	B
Q6	B
Q7	D
Q8.	B
Q9.	C
Q10.	B
Q11.	A
Q12.	A
Q13.	B
Q14.	D
Q15.	B
Q16.	D
Q17.	D
Q18.	C
Q19.	A
Q20.	D