University of Mumbai

Examination June 2021

Examinations Commencing from 1st June 2021

Program: **Information Technology**

Curriculum Scheme: Rev2019

Examination: BE Semester IV

Course Code:ITC405 and Course Name: Computer Organization & Architecture

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Memory mapped I/O means
Option A:	Using separate memory address space for I/O ports
Option B:	Assigning a part of the main memory address space to I/O ports
Option C:	Using separate input and output instructions
Option D:	Using combined input and output instructions
2.	Instruction AND is executed by
Option A:	Decoder unit
Option B:	ALU
Option C:	Memory unit
Option D:	Control unit
3.	In memory Hierarchy which is the fastest memory
Option A:	SRAM
Option B:	DRAM
Option C:	Register
Option D:	Cache
4.	Cache memory is also known as
Option A:	Content Addressable Memory
Option B:	Content Accessible Memory
Option C:	Computer Addressable Memory
Option D:	Computer Accessible Memory
5.	Micro program consisting of _____ is stored in control memory of control unit
Option A:	Instructions
Option B:	micro instructions
Option C:	micro program
Option D:	macro program
6.	Choose appropriate sequence of instruction cycle
Option A:	Instruction fetch, Instruction address calculation, Instruction decode, operand address calculation , fetch operand, data operation, operand address calculation, operand store

Option B:	Instruction address calculation , Instruction fetch, operand address calculation fetch operand, Instruction decode, data operation, operand address calculation and operand store
Option C:	Instruction address calculation , Instruction fetch, Instruction decode, operand address calculation , fetch operand, data operation , operand address calculation, operand store
Option D:	Instruction address calculation, Instruction fetch, Instruction decode, operand address calculation , fetch operand, operand address calculation , operand store, data operation
7.	In Instruction Pipelining Structural Hazard means
Option A:	any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline
Option B:	a delay in the availability of an instruction causes the pipeline to stall
Option C:	the situation when two instructions require the use of a given hardware resource at the same time.
Option D:	When a data gets overwritten by branching
8.	Convert number(41.62)$_8$ into equivalent hexadecimal number
Option A:	(20.D8)$_{16}$
Option B:	(21.C8)$_{16}$
Option C:	(21.D8)$_{16}$
Option D:	(20.C8)$_{16}$
9.	The sign and magnitude representation for +7 is
Option A:	00001000
Option B:	10000101
Option C:	10000111
Option D:	00000111
10.	8086 has 20 bit address lines to access memory, hence it can access
Option A:	100 MB
Option B:	1 KB
Option C:	1 MB
Option D:	10 MB
11.	The advantage of DMA is
Option A:	Avoiding busy waiting by CPU
Option B:	High speed data transfer between memory and I/O
Option C:	Polling
Option D:	Accessing CPU
12.	Program Counter Holds
Option A:	The Instruction
Option B:	The Data
Option C:	Address of the Current Instruction which is executed
Option D:	Address of the Next Instruction to be executed
13.	Which of the following is not a key characteristics of memory devices or memory system

Option A:	Location
Option B:	Physical Characteristics
Option C:	Availability
Option D:	Access Method
14.	In restoring division method when subtraction is said to be unsuccessful
Option A:	if result is positive
Option B:	if result is negative
Option C:	if result is zero
Option D:	if result is infinite
15.	The disadvantage of an SRAM is
Option A:	Very high power consumption
Option B:	Very high access time
Option C:	These are volatile memories
Option D:	Very low price
16.	The main memory contains 8K blocks, each consisting of 128 words. How many bits are there in a main memory address?
Option A:	19 bits
Option B:	21 bits
Option C:	22 bits
Option D:	20 bits
17.	In Restoring division Algorithm if A<0 then which of the following is immediate step (Assume M as Dividend Q as Divisor And A as result)
Option A:	Q_0 =0
Option B:	A= A +M
Option C:	Q_0 =0 & A=A-M
Option D:	Q_0 =0 & A=A+M
18.	Third generation of computer is between
Option A:	1940 and 1956
Option B:	1964 and 1971
Option C:	1972 and 2010
Option D:	1910 and 1930
19.	Find the output of full adder with A=1, B=0, C=1
Option A:	S=0,C=0
Option B:	S=0,C=1
Option C:	S=1,C=0
Option D:	S=1,C=1
20.	A combinational logic circuit which sends data coming from a single source to two or more separate destinations is
Option A:	MUX
Option B:	ENCODER
Option C:	DECODER
Option D:	DEMUX

Q2 **(20 Marks)**	***Solve any Four out of Six 5 marks each***
A	Explain the working of 8:1 Multiplexer.
B	Minimize the following four variable logic function using K-map f(A,B,C,D)=∑m(0,1,3,4,7,9,11,13,15)
C	Describe Flynn's classification of parallel computing in detail
D	Differentiate between Hardwired control unit and Micro programmed control unit
E	Identify the addressing modes of the following instructions 1.MOV AX,1000 2.MOV AX,[1000] 3.MOV AX,BX 4.MOV [BX],AX 5.MOV AX,[SI+200]
F	Write short note on DMA

Q3. **(20 Marks)**	***Solve any Two Questions out of Three 10 marks each***
A	Draw the flow chart of Booths algorithm for signed multiplication and Perform 7 x -3 using booths algorithm
B	Explain in detail with suitable Architecture of 8086 microprocessor
C	List and explain in detail characteristics /parameters of memory

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	B
Q3.	C
Q4	A
Q5	B
Q6	C
Q7	C
Q8.	B
Q9.	D
Q10.	C
Q11.	B
Q12.	D
Q13.	C
Q14.	A
Q15.	C
Q16.	D
Q17.	D
Q18.	B
Q19.	B
Q20.	D