University of Mumbai

Examination 2020 under cluster __(Lead College: _____)

Examinations Commencing from 15h June to 26th June 2021

Program: Computer Engineering

Curriculum Scheme: Rev2019

Examination: SE Semester III(for Direct Second Year-DSE)

Course Code: CSC304

Course Name: Digital Logic & Computer Organization and Architecture

Time: 2 hour Max. Marks: 80

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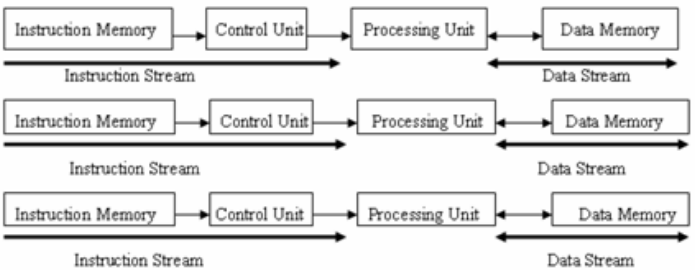
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	What is the Function of MAR
Option A:	Read/write a word form memory
Option B:	Specify an address of memory
Option C:	Contains the 8 bit opcode
Option D:	Store address of next instruction
2.	What is does the Instruction Register holds
Option A:	It Holds the Address of the Current Instruction
Option B:	It Holds the Address of the Next Instruction
Option C:	It Holds the Current Instruction
Option D:	It Holds the Next Instruction
3.	What will be the Value stored in Register A & Q of Booths Algorithm if we multiply 5 & -6
Option A:	00011110
Option B:	11100001
Option C:	11100010
Option D:	11100011
4.	The normalized form of 100001111.001 is
Option A:	1.00001111001 x 2 raise to -8
Option B:	1.00001111001 x 2 raise to 8
Option C:	0. 100001111001 x 2 raise to 9
Option D:	1.00001111001 x 2 raise to 9
5.	In Restoring division Algorithm if A<0 then which of the following is immediate step (Assume M as Dividend Q as Divisor And A as result)
Option A:	Q0 =0
Option B:	A= A +M
Option C:	Q0 =0 & A=A-M
Option D:	Q0 =0 & A=A+M
6.	Which of the following statement is true about D-Flip Flop

Option A:	The output is Complement of Input
Option B:	The output continues to remain in previous state
Option C:	The output Follows the D-Input
Option D:	The output is always high irrespective of D-input
7.	Identify which of the following is not a valid Addressing Mode
Option A:	Register Addressing mode
Option B:	Direct Addressing mode
Option C:	Register Opcode Addressing mode
Option D:	Stack Addressing Mode
8.	State table method is the method for designing
Option A:	Microprogram Control unit
Option B:	Hardwired Control Unit
Option C:	Memory Unit
Option D:	I/O devices
9.	Basic task for control unit is
Option A:	to perform logical operations
Option B:	to perform execution
Option C:	to initiate the resources
Option D:	to decode instructions and generate control signal
10.	The micro instruction MAR<--PC is executed to
Option A:	fetch the data
Option B:	fetch the instruction
Option C:	Fetch both data and instruction
Option D:	Send control signals
11.	In micro programmed control unit, micro instructions are stored in special memory called
Option A:	Control Memory
Option B:	RAM
Option C:	ROM
Option D:	Micro memory
12.	Which of the following is not a key characteristics of memory devices or memory system
Option A:	Location
Option B:	Physical Characteristics
Option C:	Availability
Option D:	Access Method
13.	Which is not true about Register memory
Option A:	fastest possible access
Option B:	only hundreds of bytes in size
Option C:	Very Large in Capacity
Option D:	Part of the processor
14.	Cache memory is implemented using

Option A:	Dynamic RAM
Option B:	Static RAM
Option C:	EPROM
Option D:	PROM
15.	The correspondence between the main memory blocks and those in the cache is given by .
Option A:	Mapping function
Option B:	Hash function
Option C:	Locale function
Option D:	Assign function
16.	In a Pipelined Processing System The Instruction $A \leftarrow 3 + A$ $B \leftarrow 4 \times A$ Leads Hazard
Option A:	Resource Hazard
Option B:	Structural Hazard
Option C:	Data Hazard
Option D:	Branch Hazard
17.	In Instruction Pipelining Structural Hazard means
Option A:	any condition in which either the source or the destination operands of an instruction are not available at the time expected in the pipeline
Option B:	a delay in the availability of an instruction causes the pipeline to stall
Option C:	the situation when two instructions require the use of a given hardware resource at the same time.
Option D:	When a data gets overwritten by branching
18.	Flynn's taxonomy classifies computer architectures based on
Option A:	the number of instructions that can be executed
Option B:	how they operate on data.
Option C:	the number of instructions that can be executed and how they operate on data.
Option D:	The number of Control Signals Generated
19.	Identify the Type of Flynn's Classification of Parallel Processing shown below 
Option A:	SISD
Option B:	SIMD
Option C:	MISD
Option D:	MIMD
20.	We can expand the processor bus connection by using
Option A:	SCSI bus

Option B:	PCI bus
Option C:	Controllers
Option D:	Multiple bus

Q2 **(20 Marks)**	**Solve any Four out of Six (5 marks each)**
A	Differentiate between Computer Organization and Architecture with a example
B	Explain any five addressing Modes with examples
C	Define Instruction cycle. Explain it with a detailed state diagram.
D	Explain Hardwired control unit design method (state table method)
E	Differentiate between Hardwired control unit and Micro programmed control unit
F	Explain the different types of Bus Arbitration methods.

Q3. **(20 Marks)**	**Solve any Two Questions out of Three (10 marks each)**
A	Consider a Cache memory of 16 words. Each block consists of 4 words. Size of the main memory is 128 bytes. Draw the Associative Mapping and Calculate the TAG and WORD size.
B	Draw the flowchart of Restoring Division Algorithm & perform 7 / 3 using this Algorithm
C	Write short note on Flynn's classification

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	C
Q3.	C
Q4	B
Q5	D
Q6	C
Q7	C
Q8.	B
Q9.	D
Q10.	B
Q11.	A
Q12.	C
Q13.	C
Q14.	B
Q15.	A
Q16.	C
Q17.	C
Q18.	C
Q19.	D
Q20.	B