University of Mumbai
Examination 2021 under Cluster 06
(Lead College: Vidyavardhini's College of Engg Tech)

Examination for Direct Second Year Students Commencing from 10th April 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III (For DSE Students)

Course Code: ELC303 and Course Name: Digital Logic Circuits

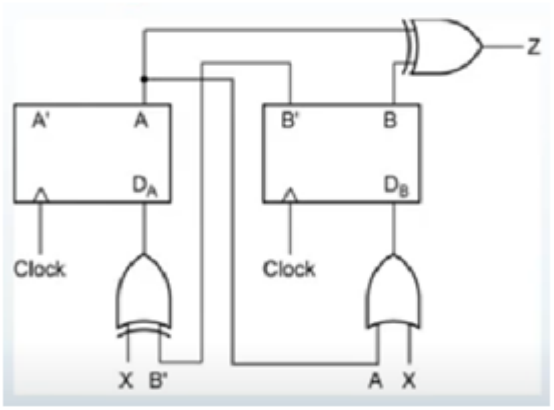
Time: 2 hour Max. Marks: 80

Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Convert Decimal$(105)_{10}$ to Binary
Option A:	$(101001)_2$
Option B:	$(1101001)_2$
Option C:	$(1110101)_2$
Option D:	$(1001011)_2$
2.	In Hamming code, which expression will help you to find out the number of parity bits.
Option A:	$2^P>=P+M+1$
Option B:	$2^P<=P+M+1$
Option C:	$2^P=P+M-1$
Option D:	$2^P<=P+M-1$
3.	What is the reflected binary code of $(100101)_2$.
Option A:	111000
Option B:	101010
Option C:	101111
Option D:	110111
4.	A multiplexer with 3 select lines is a
Option A:	4:1 multiplexer
Option B:	8:1 multiplexer
Option C:	16:1 multiplexer
Option D:	32:1 multiplexer
5.	IC 74138 is a
Option A:	3:8 line decoder
Option B:	1:8 line decoder
Option C:	4:8 line decoder
Option D:	any lines to 8 line decoder
6.	Which of the following ICs can be used as a comparator?
Option A:	IC7408
Option B:	IC7400

Option C:	IC7485
Option D:	IC7420
7.	In which type of machine the output depends on the present state and external input.
Option A:	Mealy machine
Option B:	Sequential asynchronous machine
Option C:	Asynchronous machine
Option D:	Moore machine
8.	IC 7492 is a
Option A:	MOD 12 Asynchronous counter
Option B:	MOD 12 Synchronous counter
Option C:	MOD 16 Asynchronous counter
Option D:	MOD 16 Synchronous counter
9.	Which of the following is a decade counter?
Option A:	IC 7493
Option B:	IC 7490
Option C:	IC 7491
Option D:	IC 7492
10.	Which one of the following methods can be used for state reduction?
Option A:	K-Maps
Option B:	Implication Chart method
Option C:	Truth Table
Option D:	Quine Mcclusky method
11.	Which of the given logic family dissipates minimum power
Option A:	TTL
Option B:	CMOS
Option C:	DTL
Option D:	ECL
12.	IC 74194 is a
Option A:	Ring counter
Option B:	4-bit bidirectional universal shift register
Option C:	Unidirectional shift register
Option D:	4-bit register
13.	What does FPGA stand for
Option A:	Field Programming Gate Array
Option B:	Field Programmable Gate Array
Option C:	First Program Gate Array
Option D:	First Programmable Gate Array
14.	Programmable Array Logic has
Option A:	a programmable AND and fixed OR array
Option B:	a programmable AND and a programmable OR array

Option C:	only a programmable AND array
Option D:	only a programmable OR array
15.	The number of similar gates which can be driven by a gate is called as_____
Option A:	Power dissipation
Option B:	Noise margin
Option C:	Fan-out
Option D:	Speed
16.	A CPLD device consist of
Option A:	PAL-Like Blocks, I/O blocks, and a set of interconnection wires
Option B:	PLA-Like Blocks and I/O blocks
Option C:	FPGAs
Option D:	Only interconnecting wires
17.	Which type of modeling style is not used in verilog hardware description language
Option A:	Structural
Option B:	Datatype
Option C:	Behavioral
Option D:	Data Flow
18.	_____ is a net data type used in Verilog.
Option A:	reg
Option B:	integer
Option C:	real
Option D:	wire
19.	Register data type in Verilog HDL is denoted as
Option A:	reg
Option B:	register
Option C:	RG
Option D:	wire
20.	Comment lines in Verilog HDL is denoted by
Option A:	//
Option B:	\
Option C:	\\
Option D:	*

Q2 **(20 Marks)**	
A	**Solve any Two 5 marks each**
i.	Explain with neat diagrams working of IC7483
ii.	State the differences between mealy and moore machine.
iii.	Write a short note on Complex Programmable Logic Devices.

B	**Solve any One 10 marks each**
i.	Design a MOD-6 counter using IC7490.
ii.	Write a program using Verilog HDL to implement a 8:1 multiplexer.
Q3 **(20 Marks)**	
A	**Solve any Two 5 marks each**
i.	Explain with suitable diagrams working of IC74163.
ii.	Write a program using Verilog HDL for implementing a half adder.
iii.	Explain in brief about the interfacing of CMOS to TTL ICs.
B	**Solve any One 10 marks each**
i.	Write a short note on carry look ahead adder.
ii.	Analyze the given state machine and draw the state diagram. 

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Q1:

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	B
Q2.	A
Q3.	D
Q4	B
Q5	A
Q6	C
Q7	A
Q8.	A
Q9.	B
Q10.	B
Q11.	B
Q12.	B
Q13.	B
Q14.	A
Q15.	C
Q16.	A
Q17.	B
Q18.	D
Q19.	A
Q20.	A

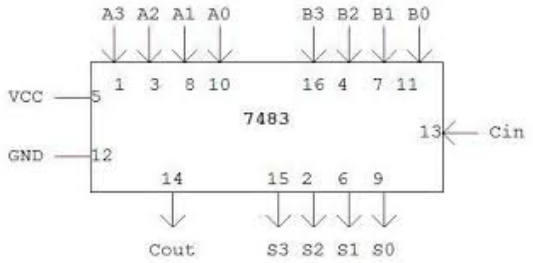
Important steps and final answer for the questions involving numerical example

Q2(A):

(i)IC7483 4 bit Binary Adder

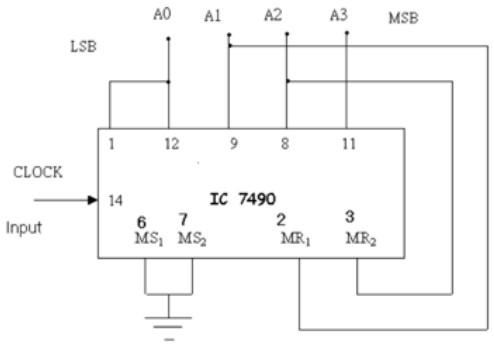
- IC 7483 –Four bit Binary Adder IC
- 4 bit Binary Number A ,4 bits are A3,A2,A1,A0
- 4 bit Binary Number B, 4 bits are B3,B2,B1,B0
- Cin, Cout

Sum we will get at S3,S2,S1,S0



Q2B(i) Asynchronous BCD Decade counter IC 7490

Set pins are active low and reset pins are active high



Q2B(ii)

```
module Mulitplexer(d0,d1,d2,d3,d4,d5,d6,d7,sel,out);
    input d0,d1,d2,d3,d4,d5,d6,d7;
    input [2:0] sel;
    output reg out;
    always@(sel)
    begin
        case(sel)
            3'b000:out=d0;
            3'b001:out=d1;
            3'b010:out=d2;
            3'b011:out=d3;
            3'b100:out=d4;
            3'b101:out=d5;
            3'b110:out=d6;
            3'b111:out=d7;
        endcase
    end
endmodule
```

Q3A(ii)

module HalfAdder (A, B, Sum Carry);
input A, B;
output Sum, Carry;
assign Sum = A ^ B; //^denotes XOR
assign Carry = A & B; //& denotes AND
endmodule

Q3B(ii)

Step1:Moore machine

Step2 :Equations

$A^+ = D_A = X \oplus B'$

$B^+ = D_B = A+X$

Z=A XOR B

Step3:State transition table

Present State AB	Input X	Next State A^+B^+	Current Output Z
00	0	10	0
	1	01	
01	0	00	1
	1	11	
10	0	11	1
	1	01	
11	0	01	0
	1	11	

Step 4: State assignment

S_0=00, S_1=01,S_2=10,S_3=11

Step 5: State Diagram