

**University of Mumbai**  
**Examination 2021 under Cluster 06**  
**(Lead College: Vidyavardhini's College of Engg Tech)**

**Examination for Direct Second Year Students Commencing from 10<sup>th</sup> April 2021**

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III (For DSE Students)

Course Code: ELC302 and Course Name: Electronic Devices and Circuits I

Time: 2 hour

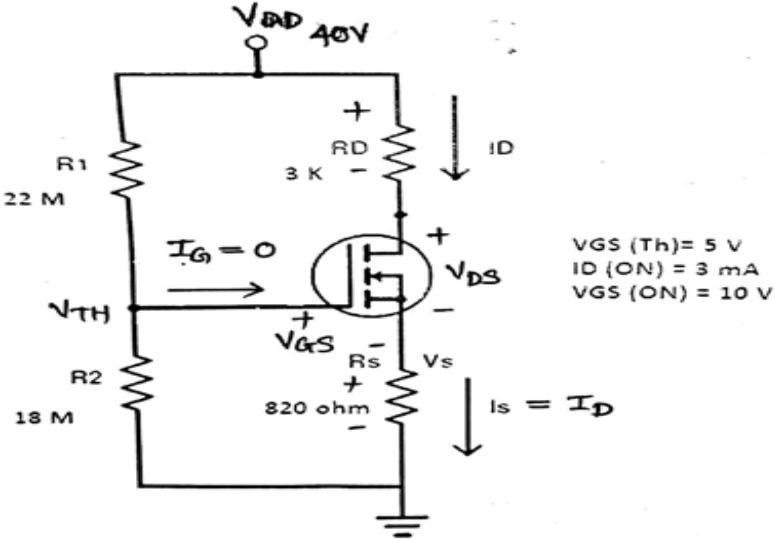
Max. Marks: 80

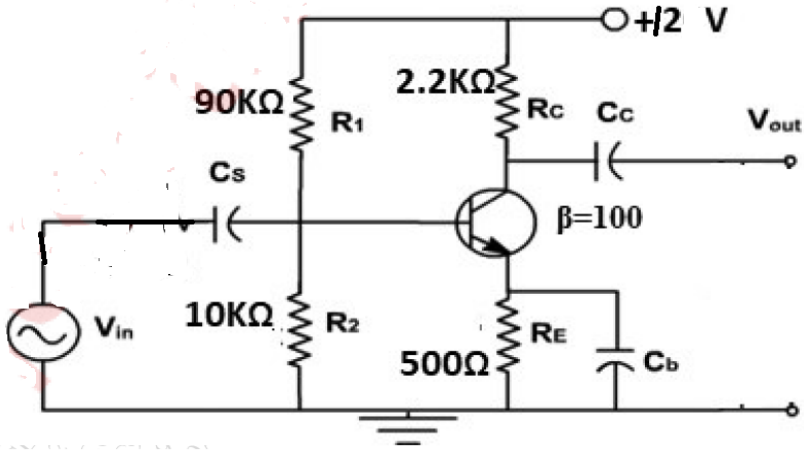
Q1.	<b>Choose the correct option for following questions. All the Questions are compulsory and carry equal marks</b>
1.	Fermi energy level for n-type semiconductors lies -----and P type semiconductor lies -----
Option A:	Close to conduction band , Close to valence band
Option B:	Close to conduction band , Close to conduction band
Option C:	Close to valence band , Close to conduction band
Option D:	Close to valence band, Close to valence band
2.	In any semiconductor material, the drift current is proportional to
Option A:	Concentration gradient of charge carriers
Option B:	Square of applied electric field
Option C:	Applied electric field
Option D:	Cube of applied electric field
3.	In fixed bias circuit using an NPN transistor, if $V_{CC} = 12V$ , $V_{BE} = 0.7V$ , Base resistor $R_B = 240\ k$ then $I_B$ is
Option A:	80 $\mu A$
Option B:	47 $\mu A$
Option C:	50 $\mu A$
Option D:	130 mA
4.	H parameter model consists of components such as
Option A:	small signal resistance $r_{pi}$ and a dependent current source $g_m V_{pi}$
Option B:	input impedance, reverse voltage gain, current gain and output conductance
Option C:	small signal resistance $r_e$ and a controlled current source
Option D:	small signal resistance $r_{pi}$ and an independent current source $g_m V_{pi}$
5.	Which Configuration has a high input impedance and low output impedance
Option A:	Common Collector Configuration
Option B:	Common Base Configuration
Option C:	Common Emitter Configuration
Option D:	Collector Base Configuration
6.	In a bipolar junction transistor (BJT) if $\beta = 100$ & collector current ( $I_C$ ) is 0.93 mA then what is the value of base current ( $I_B$ ) ?
Option A:	9.3 $\mu A$
Option B:	0.93 $\mu A$

Option C:	93 $\mu$ A
Option D:	93 mA
7.	To operate transistor in its forward active / linear mode of operation base emitter junction is ----- and the collector base junction is -----
Option A:	reverse biased, forward biased
Option B:	reverse biased, reverse biased
Option C:	forward biased ,reverse biased
Option D:	forward biased, forward biased
8.	The voltage gain of a common base amplifier is
Option A:	Zero
Option B:	Less than unity
Option C:	Unity
Option D:	Greater than unity
9.	The relation between $\alpha$ and $\beta$ is
Option A:	$\alpha = (1+\beta) / \beta$
Option B:	$\alpha = \beta / (1+\beta)$
Option C:	$\alpha = \beta / (1- \beta)$
Option D:	$\alpha = (1-\beta) / \beta$
10.	In case of DMOSFET drain current $I_D$ depends upon
Option A:	V <sub>DD</sub>
Option B:	I <sub>G</sub>
Option C:	V <sub>GS</sub>
Option D:	I <sub>S</sub>
11.	For E-MOSFETs, the relationship between output current and controlling voltage is defined by-----.
Option A:	$I_D = k [(V_{GS} - V_{GS(Th)})]^2$
Option B:	$I_D = k [(V_{GS} - V_{SB})]^2$
Option C:	$I_D = k [(V_{GS} - V_{DS})]^2$
Option D:	$I_D = k [(V_{GS} - V_{GS(Th)})]^2$
12.	The N channel connecting two N regions is absent in
Option A:	N channel DMOSFET
Option B:	N channel EMOSFET
Option C:	P channel DMOSFET
Option D:	P channel EMOSFET
13.	The biasing method used for EMOSFET are voltage divider biasing circuit and---
Option A:	self bias circuit
Option B:	fixed bias
Option C:	collector to base bias circuit
Option D:	feedback biasing circuit
14.	The input impedance of the MOSFET is very high .Give reason
Option A:	The SiO <sub>2</sub> layer is present between gate terminal and channel.
Option B:	Metallic contacts are used for connecting the Drain, gate and source terminals

Option C:	A P type semiconductor is used as a substrate.
Option D:	A N type semiconductor is used as a substrate.
15.	A common drain amplifier has voltage gain
Option A:	Slightly less than 1.
Option B:	Greater than 1
Option C:	Infinite
Option D:	Zero
16.	Input signal of common source amplifier is applied to
Option A:	Source terminal
Option B:	Gate terminal
Option C:	Drain terminal
Option D:	Substrate terminal
17.	Phase difference between input and output of a source follower circuit is
Option A:	0 degree
Option B:	90 degrees
Option C:	180 degrees
Option D:	45 degrees
18.	For the CS amplifier circuit calculate voltage gain $A_v$ if $g_m = 200 \text{ micro A/V}$ and $R_D = 14K\Omega$
Option A:	-2.8
Option B:	2.8
Option C:	4.8
Option D:	-4.8
19.	Reactance of capacitor is given by
Option A:	$X_c = 1/2 \pi f C$
Option B:	$X_c = 1/2 \pi R C$
Option C:	$X_c = 1/2 \pi L C$
Option D:	$X_c = 1/2 \pi R L$
20.	In the design steps for RC coupled CE amplifiers, the voltage drop across emitter resistor $R_E$ should be ----- as compared to base emitter voltage of transistor
Option A:	lower
Option B:	higher
Option C:	same
Option D:	Zero

<b>Q2.</b> <b>(20 Marks )</b>	
<b>Q.2 A)</b>	<b>Solve any two out of three (5 marks each)</b>
i.	Draw Energy band diagram of PN junction diode under Forward biased, Reverse biased and Zero biased.
ii.	Compare CE, CB, CC Configurations of BJT.
iii.	Explain hybrid $\pi$ model of BJT.
<b>Q2. B)</b>	<b>Solve any One Question out of two. (10 marks each)</b>
i.	Design a single stage RC Coupled CE amplifier using transistor with given specifications as $ A_v =70$ , $V_o \text{ rms}=4.5\text{V}$ , $F_L=10 \text{ Hz}$ , $V_{CE(\text{SAT})}=1\text{V}$ , $h_{fe}=180$ , $h_{ie}=2.7\text{K}\Omega$ and $S < 8$ .
ii.	Draw the neat diagram of voltage divider biased CS MOSFET amplifier and source resistance bypass and derive the expression for the voltage gain.

<b>Q3).</b> <b>(20 Marks )</b>	<b>Solve any Two Questions out of Three (10 marks each)</b>
A	 <p style="text-align: center;">Fig.1</p> <p>For the voltage divider bias circuit shown in Fig. 1 using N-channel E-MOSFET, <math>V_{DD}=40\text{V}</math>, <math>V_{GS(\text{TH})}=5\text{V}</math>, <math>I_{D(\text{ON})}=3 \text{ mA}</math> and <math>V_{GS(\text{ON})}=10\text{V}</math>. Calculate Q - point where <math>Q = [V_{DSQ}, I_{DQ}]</math>.</p>

<p>B</p>	 <p style="text-align: center;">Fig. 2</p> <p><math>R_1=90\text{K}\Omega</math>, <math>R_2=10\text{K}\Omega</math>, <math>V_{CC}=12\text{V}</math>, <math>\beta=100</math>, <math>V_{BE}=0.7\text{V}</math>, <math>R_C=2.2\text{K}\Omega</math>, <math>R_E=500\Omega</math></p> <p>Find out voltage gain <math>A_v</math>, input impedance <math>R_i</math> and output impedance <math>R_o</math> for the given circuit in Fig. 2</p>
<p>C</p>	<p>Design a single stage RC Coupled CE amplifier using transistor with following specifications.</p> <p><math>h_{fe}=220</math>, <math>h_{ie}=2.7\text{K}\Omega</math>, <math> A_v =180</math>, <math>S=10</math>, <math>V_o=3\text{V}</math>, <math>V_{CC}=18\text{V}</math>,  <math>F_L=20\text{Hz}</math>, <math>V_{CE(SAT)}=1\text{V}</math></p>

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**Q1:**

<b>Question Number</b>	<b>Correct Option (Enter either 'A' or 'B' or 'C' or 'D')</b>
Q1.	A
Q2.	C
Q3.	B
Q4	B
Q5	A
Q6	A
Q7	C
Q8.	D
Q9.	B
Q10.	C
Q11.	D
Q12.	B
Q13.	D
Q14.	A
Q15.	A
Q16.	B
Q17.	A
Q18.	A
Q19.	A
Q20.	B

## Important steps and final answer for the questions involving numerical example

### Question number.3 A) SOLUTION

Q.3 A) find  $I_D$ ,  $V_{DSQ}$

$V_{gs(TH)} = 5V$   
 $I_{D(on)} = 3mA$   
 $V_{gs(on)} = 10V$

① find  $K$

$$K = \frac{I_{D(on)}}{[V_{gs(on)} - V_{gs(TH)}]^2} = \frac{3 \times 10^{-3}}{[10 - 5]^2} = 1.2 \times 10^{-4} A/V^2$$

② find  $I_D$

$$I_D = K [V_{gs} - V_{gs(TH)}]^2$$

but  $V_{gs} = V_G - V_S$

$$V_G = \frac{R_2}{R_1 + R_2} \times V_{DD} - I_D R_S$$

$$= \frac{18}{18 + 22} \times 40 - 820 I_D$$

$$\therefore I_D = 1.2 \times 10^{-4} [18 - 820 I_D - 5]^2$$

$$I_D = 6.69 mA \text{ or } 37.4 mA$$

select  $I_D = 6.69 mA$

③ find  $V_{DSQ}$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

$$= 40 - 6.69 \times 10^{-3} (3 \times 10^3)$$

$$= 14.44 V$$

### Question number.3 B SOLUTION

Q.3 B

Given  $R_1 = 90K, R_2 = 10K$   
 $R_3 = 2.2K, R_4 = 500$   
 $V_{gs(TH)} = 5V$   
 $I_{D(on)} = 3mA$   
 $V_{gs(on)} = 10V$   
 $\beta = 100$

find  $A_V, R_i^o \& R_o$

$$V_{th} = \frac{R_2}{R_1 + R_2} \times V_{CC} = \frac{10K}{90K + 10K} \times 12 = 1.2V$$

$$R_{th} = R_1 || R_2 = 90K || 10K = 9K$$

① find  $I_B$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + \beta) R_E} = \frac{1.2 - 0.7}{9K + (101)0.5K} = 8.44 \mu A$$

$$I_C = \beta I_B = 100 \times 8.44 \times 10^{-6} = 0.844 mA$$

② AC analysis

$$\gamma_{\pi} = \frac{V_T \times \beta}{I_C} = \frac{26mV \times 100}{0.844 \times 10^{-3}} = 3.095 k\Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{0.844 mA}{26mV} = 32.3 \frac{mA}{V}$$

Hybrid  $\pi$  equivalent ckt

$R_i^o = \gamma_{\pi} = 3.095 k\Omega$   
 $R_i^i = R_{th} || \gamma_{\pi} = 9K || 3.095 k\Omega = 2.3 k\Omega$   
 $A_V = -g_m R_C = -32.3 \times 2.2 = -71.06$   
 $R_o = R_C = 2.2 k\Omega$