University of Mumbai

Examination June 2021

Examinations Commencing from 15th June 2021 to 26th June 2021

Program: **Bachelor of Engineering**

Curriculum Scheme: **Electronics & Telecommunication (Rev2019 'C' Scheme)**

Examination: **DSE** Semester **III**

Course Code: **ECC303** and Course Name: **Digital System Design**

Time: 2 hour Max. Marks: 80

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Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.**
1.	Convert binary number into gray code: 100101.
Option A:	101101
Option B:	001110
Option C:	110111
Option D:	111001
2.	The representation of octal number (532.2)8 in decimal is
Option A:	(346.25)10
Option B:	(532.864)10
Option C:	(340.67)10
Option D:	(531.668)10
3.	The octal number (651.124)8 is equivalent to
Option A:	(1A9.2A)16
Option B:	(1B0.10)16
Option C:	(1A8.A3)16
Option D:	(1B0.B0)16
4.	How many AND gates are required to realize Y = CD + EF + G?
Option A:	4
Option B:	5
Option C:	3
Option D:	2
5.	Which of the following is not a basic gate?
Option A:	AND
Option B:	OR
Option C:	EXOR
Option D:	NOT
6.	A(A + B) = ?
Option A:	AB
Option B:	1
Option C:	(1 + AB)
Option D:	A

7.	A Karnaugh map (K-map) is an abstract form of _____ diagram organized as a matrix of squares.
Option A:	Venn Diagram
Option B:	Cycle Diagram
Option C:	Block diagram
Option D:	Triangular Diagram
8.	Odd parity of word can be conveniently tested by
Option A:	OR gate
Option B:	AND gate
Option C:	NAND gate
Option D:	XOR gate
9.	If A and B are the inputs of a half adder, the sum is given by _____
Option A:	A AND B
Option B:	A OR B
Option C:	A XOR B
Option D:	A EX-NOR B
10.	The output of a subtractor is given by (if A, B and X are the inputs).
Option A:	A AND B XOR X
Option B:	A XOR B XOR X
Option C:	A OR B NOR X
Option D:	A NOR B XOR X
11.	The addition of two decimal digits in BCD can be done through _____
Option A:	BCD adder
Option B:	Full adder
Option C:	Ripple carry adder
Option D:	Carry look ahead
12.	Which of the following is correct for a D-type flip-flop?
Option A:	The output follows the D input with each clock pulse.
Option B:	The output complement follows the D input with each clock pulse
Option C:	The output remains HIGH all the time
Option D:	The output toggles with each clock pulse
13.	In a Master Slave flip flop the output is taken
Option A:	from the Master
Option B:	from the Slave
Option C:	from Master output ANDED with Slave output
Option D:	from Master output ORED with Slave output
14.	How can parallel data be taken out of a shift register simultaneously?
Option A:	Use the Q output of the first FF
Option B:	Use the Q output of the last FF
Option C:	Tie all of the Q outputs together
Option D:	Use the Q output of each FF

15.	PLA is used to implement
Option A:	A complex sequential circuit
Option B:	A simple sequential circuit
Option C:	A complex combinational circuit
Option D:	A simple combinational circuit
16.	VHDL is being used for
Option A:	Documentation only
Option B:	Verification only
Option C:	Synthesis only of digital design
Option D:	Documentation, Verification and Synthesis of digital design
17.	Where do we declare the loop index of a FOR LOOP?
Option A:	Entity
Option B:	Architecture
Option C:	Library
Option D:	It doesn't have to be declared
18.	In delay flip-flop, _____ after the propagation delay.
Option A:	Input follows input
Option B:	Input follows output
Option C:	Output follows input
Option D:	Output follows output
19.	Comparators are used in
Option A:	Memory
Option B:	CPU
Option C:	Motherboard
Option D:	Hard drive
20.	A magnitude comparator is defined as a digital comparator which has
Option A:	Only one output terminal
Option B:	Two output terminals
Option C:	Three output terminals
Option D:	No output terminal

Q2.	**Answer the following :**
A	**Solve any Two** **5 marks each**
i.	State and prove Demorgan's theorem.
ii.	Compare PAL with PLA .
iii.	Perform the following operation using 2's complement. i) $(14)_{BASE\ (10)} - (24)_{BASE\ (10)}$ ii) (24)BASE (10)− (14)BASE (10)
B	**Solve any One** **10 marks each**
i.	Minimize the following expression using Quine MC-cluskey technique. $F(A, B, C, D) = \sum M(0,1,2,3,5,7,9,11)$
ii.	Prove that NAND and NOR gates are universal gates.

Q3.	**Answer the following:**
A	**Solve any Two** **5 marks each**
i.	Write the VHDL code for a full subtractor.
ii.	Convert SR Flip flop to JK Flip flop.
iii.	Design 3 bit full adder circuit and explain in detail.
B	**Solve any One** **10 marks each**
i.	What are shift registers? How are they classified? Explain working of any type of shift register.
ii.	Draw and explain a neat circuit diagram of BCD adder .

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	A
Q3.	A
Q4.	D
Q5.	C
Q6.	D
Q7.	A
Q8.	D
Q9.	C
Q10.	B
Q11.	A
Q12.	A
Q13.	B
Q14.	D
Q15.	C
Q16.	D
Q17.	D
Q18.	C
Q19.	B
Q20.	C