K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
End Semester Exam
Nov – Dec 20-21
(B.Tech/M.Tech.) Program: B.Tech
Examination: SY Semester: III
Course Code: 1UEXC302 and Course Name: Digital Logic Design
Duration: 03 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Difference Between Mealy And Moore Machine	02	4	U
ii)	What Is The Difference Between CMOS and TTL? Which one is Better?	02	1	U
iii)	State De Morgan's theorem	02	1	R
iv)	Convert the given expression in canonical SOP form Y = AC + AB + BC	02	2	App
v)	What are the application of ROM and PROM memories?Explain	02	3	U
vi)	Explain the flip-flop excitation tables for RS FF.	02	4	U
vii)	Write the names of different modelling of VHDL	02	6	R
viii)	Write down the features of FPGA	02	5	R

Q.2	**Solve any four questions out of six.**	**16**		
i)	Draw and explain a neat circuit diagram of BCD adder.	04	1	App
ii)	Minimize the following expression using Quine Mc-cluskey techniques F(A,B,C,D)=M(0,1,2,3,5,7,9,11)	04	2	App
iii)	Compare SRAM with DRAM	04	3	U
iv)	Explain Master-Slave S-R flip-flop.	04	4	U
v)	Compare PAL with PLA	04	5	U
vi)	Write VHDL code for Fibonacci series Generator sequential circuit.	04	6	App
Q.3	**Solve any two questions out of three.**	**16**		
i)	Prove that NAND and NOR gates are Universal gates.	08	1	App
ii)	Explain the working of a master-slave JK flip-flop with the help of logic diagram, function table, logic symbol and timing diagram.	08	4	U
iii)	Design Full adder using PLA	08	5	App
Q.4	**Solve any two questions out of three.**	**16**		
i)	Demonstrate the access time of PROM with timing diagram	08	3	U
ii)	Implement following Boolean function using 8:1 multiplexer $F(A,B,C,D)=\bar{A}B\bar{D}+ACD+\bar{B}CD+\bar{A}\bar{C}D$	08	2	App
iii)	Explain the detail structure of VHDLModule and also explain Port modes in VHDL	08	6	U