K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
End Semester Exam
Nov – Dec 2021
(B.Tech.) Program: Electronics and Telecommunication
Examination:TY Semester: V
Course Code: 1UEXC502 and Course Name: Digital VLSI Design

Duration: 03 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Draw Stick diagram of inverter		1	U
ii)	Define Noise margin with proper equation		2	R
iii)	Define Setup time and Hold time		3	R
iv)	Draw neat circuit of 1T DRAM		4	U
v)	Define controllability and observability		5	R
vi)	Show stuck-in 0 fault with suitable example		5	A
vii)	Write 2 types of RTL design techniques give one example for each.		6	R
viii)	Draw NAND gate using Pseudo nMOS		3	A
Q.2	**Solve any four questions out of six**	**16**		
i)	Compare Full scaling and constant Voltage scaling		1	U
ii)	Draw layout of NAND gate using lambda based design rules		2	A
iii)	Implement 2:1 Multiplexor using transmission gate		3	A
iv)	Draw and Explain 3-T DRAM with neat daigram		4	U
v)	Implement carry circuit of 4 bit carry look ahead adder using Dynamic NMOS		5	A
vi)	Implement datapath of 3-TAP parallel FIR filter		6	A

Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain n-MOS fabrication process with neat and clean diagrams.		1	U
ii)	Draw layout of 6-T SRAM using lambda design rules		4	A
iii)	Implement the following data path elements 1. Sum and carry circuit for 1-Bit full adder using static CMOS 2. 4-Bit carry bypass adder		3,5	A
Q.4	**Solve any two questions out of three.**	**16**		
i)	Design soda dispenser machine using RTL Design method. Draw HLSM, DATAPATH and Interface and FSM		6	C
ii)	Implement Y = A+BC equation using following logic design styles 1. Static CMOS 2. Pseudo NMOS 3. Domino Logic 4. Dynamic PMOS		3	C
iii)	Explain CMOS inverter with Voltage Transfer characteristics. Show all regions using following voltages VIL, VOH, VIH, VOL and VTH on VTC.		2	U