K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22

(Autonomous College Affiliated to University of Mumbai)

End Semester Exam

Nov – Dec 2021

(B.Tech/M.Tech.) Program: B. Tech

Examination: DSY_ Semester: III

Course Code: 1UEXC302 and Course Name: Digital Logic Design

Duration: 03 Hours Max. Marks: 60

Instructions:

(1)All questions are compulsory.

(2)Draw neat diagrams wherever applicable.

(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Convert decimal $(163.875)_{10}$ to binary form.	02	1	U
ii)	Compare Sequential Circuits with Combinational Circuits.	02	2	U
iii)	Explain De Morgan's Theorem.	02	1	U
iv)	If F (A, B, C) = Σ m (0, 3, 5, 7), Express F in SOP form.	02	2	App
v)	What is the need of Master Slave JK flip flop?	02	4	U
vi)	How does a J-K Flip Flop differ from an S-R Flip Flop in its operation?	02	4	U
vii)	Compare Static RAM and Dynamic RAM	02	3	U
viii)	Explain 2-bit Magnitude Comparator.	02	2	App

Q.2	**Solve any four questions out of six.**	**16**		
i)	Convert T type Flip Flop into D type Flip Flop.	04	4	App
ii)	Implement 4- bit Full Adder using carry look ahead logic.	04	2	App
iii)	Add -75 and +26 using 8-bit 2's complement Arithmetic.	04	1	App
iv)	Explain Flash Memories.	04	5	U
v)	How can a NOR and NAND gates be used as an inverters?	04	1	U
vi)	Reduce the following expression using K-map and implement the real minimal expression in Universal Logic $F=\Sigma$ m (0,2,4,6,7,8,10,12,13,15)	04	2	App
Q.3	**Solve any two questions out of three.**	**16**		
i)	Minimize following expression using Quine McClusky method. $F(A, B, C, D) = \Sigma m(0, 1, 2, 3,5, 7, 9, 11)$	08	2	App
ii)	Convert $(756.603)_8$ to Hexadecimal and $(B9F.AE)_{16}$ to Octal.	08	1	App
iii)	Explain Universal Shift Register with the help of diagram.	08	4	U
Q.4	**Solve any two questions out of three.**	**16**		
i)	Implement Full Adder logic using VHDL code	08	6	App
ii)	Explain Classification of RAM and ROM Memories.	08	3	App
iii)	What are the advantages and disadvantages of using PROM as a PLD? And also compare PAL and PLA.	08	5	U