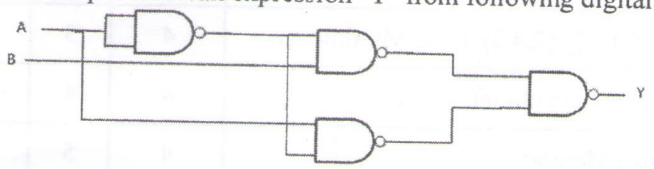
06/12/2022

K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Nov – Dec 2022
(B.Tech.) Program: Electronics and Telecommunication
Examination: SY Semester: III

Course Code: EXC302 Course Name: Digital Logic Design
Duration: 2.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	Convert Binary digit (101.11) into Decimal form.	2	1	A
ii)	Find the output Boolean expression 'Y' from following digital circuit 	2	2	U
iii)	Write SOP form of logical expression with the help of following truth table.	2	3	U
iv)	Complete the truth table for 02-input Multiplexer.	2	3	U
v)	Draw 02-bit Asynchronous Up-Counter using J-K flip flops.	2	4	U
vi)	Calculate the number of address lines require to develop a unique address for each of the 4096 memory locations.	2	5	A
vii)	List the hardware description languages for describing digital designs on CPLD and FPGA devices.	2	6	U

INPUTS		Y (Output)
A	B	
0	0	
0	1	
1	0	
1	1	

S0	I0	I1	Output
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

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viii)	For 2-bit SISO shift register data 1011 is input to first flip flop. What will be the status of output (QB) of 2nd flip flop after 04 clock cycles?	2	4	A
Q.2	Solve any four questions out of six.	16		
i)	Perform following operation using Excess-3 BCD code a) Add $(0011\ 0101\ 0110)_{BCD}$ and $(0101\ 0111\ 1001)_{BCD}$ and verify the result using equivalent decimal addition. b) Subtract $(185)_{10} - (8)_{10}$	4	1	A
ii)	Draw the logic arrangement for a) Four-input NAND gate using two-input AND gate and NOT gate. b) Calculate the number of flip flops driven by the output of inverter logic if the maximum output HIGH-state current is 1mA, the maximum output LOW-state current is 20mA, the maximum input HIGH-state current is 50uA, and The maximum input LOW-state current is 2mA.	4	2	C
iii)	Implement the Boolean function f(A,B,C) = ∑ (2,4,7) using Multiplexer.	4	3	C
iv)	Explain Switch Debouncing using NAND latch circuit.	4	4	U
v)	Compare RAM,ROM,EPROM and Flash Memory.	4	5	U
vi)	Differentiate PLA device and PAL device.	4	6	U
Q.3	Solve any two questions out of three.	16		
i)	Design 4-bit Binary to Gray converter using logic gates.	8	1	C
ii)	Draw 4-bit Ring counter and Explain its operation with the help of Timing Diagram.	8	4	C
iii)	Draw and Explain Generalize Architecture of a PAL device.	8	5	U
Q.4	Solve any two questions out of three.	16		
i)	Explain DeMorgans Theorem and Prove the following Boolean Expression. a) $A.B.C.D+A.B.\overline{C}.D+A.B.C.\overline{D}+A.B.\overline{C}.D+A.B.C.D.E+A.B.\overline{C}.\overline{D}.\overline{E}+A.B.\overline{C}.D.E = A.B$ b) $[A.\overline{B}+\overline{C}+D].[D+(E+\overline{F}).G] = D.(A.\overline{B}+\overline{C})+D.G.(E+\overline{F})$	8	2	A
ii)	Using the Quine-McClusky tabular method, Find the Minimum Sum-of-product for F(A,B,C,D) = ∑ (1,2,3,9,12,13,14) + ∑ (0,7,10,15)	8	3	A
iii)	What is VHDL? Write VHDL code for Full Adder using Structural modeling.	8	6	U

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