27-01-2023

K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22

(Autonomous College Affiliated to University of Mumbai)

End Semester Exam

Jan – Feb 2023

(B.Tech) Program: Electronics and Telecommunication

Examination: DSY Semester: III

Course Code: EXC302 and Course Name: Digital Logic Design

Duration: 03 Hours Max. Marks: 60

Instructions:

(1)All questions are compulsory.

(2)Draw neat diagrams wherever applicable.

(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	How many T flip flops required in 3 bit shift register.	02	4	U
ii)	Explain ROM.	02	3	U
iii)	In four variable K map if all minterm are present then the output will be.	02	2	U
iv)	The output of a logic gate is '0' when all its input are at logic 1.The gate is.	02	1	U
v)	Minimum number of NOR logic gates required to implement EX-NOR gate.	02	1	U
vi)	What is the Two's complement of Binary 1011.	02	1	U

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vii)	Explain flash memories.	02	3	U
viii)	Explain 1 bit memory cell.	02	3	U
Q.2	**Solve any four questions out of six.**	**16**		
i)	Implement 2:1 MUX.	04	2	App
ii)	simplify $Y=\sum m(0,1,3,5,7,10,13) + d(2,8,12)$ using K-Map.	04	3	App
iii)	Design 4 bit shift register.	04	4	App
iv)	Explain DRAM with the help of diagram.	04	3	U
v)	State the Demorgan's theorem.	04	1	U
vi)	Implement EX-NOR gate using NAND gates only.	04	1	App
Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain four bit Binary Adder using IC 7483.	08	2	U
ii)	Design three bit ring counter.	08	4	App
iii)	Write a short note on ROM and EPROM.	08	3	U
Q.4	**Solve any two questions out of three.**	**16**		
i)	Add the number using 2's compliment (a) -34 and 15 (b) 24 and -30	08	1	App
ii)	Write short notes on Programmable Logic Array (PLA), and Programmable Array Logic (PAL).	08	5	U
iii)	Write VHDL code for Subtractor circuit and also draw the waveform.	08	6	App

02/02

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Digital logic Design.

Describe the various types of registers. (2M)

Q1(v) Convert $(532.125)_8$ into binary and hexadecimal. (2M)

Q1(viii) explain types of Memory -(2M)

Q2(ii) If $(A,B,C) = \Sigma m(0,3,5,7)$ write its truth table and express f in SOP and POS form (4M)

Q3 (ii) Explain JK flip flop using NAND Gate in detail with excitation table (8M)

Q4(iii) Write VHDL code for ~~Subtractor~~ Adder circuit and also draw the waveform. (8M)