K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Subject Code:CEC304/AIC304 Subject Name: Digital Logic and Computer Architecture

Date: 01 / 02 /2023

January 2023

(B.Tech) Program: Computer Engineering/Artificial Intelligence and Data Science

Examination: DSY Semester: III

Course Code: CEC304/AIC304 and Course Name: Digital Logic and Computer Architecture

Duration: 2.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	What is Von-Neumann architecture?	02	CO1	U
ii)	Write IEEE 754 single precision floating point number format.	02	CO2	U
iii)	Write a JK flip flop truth table.	02	CO3	U
iv)	Identify Addressing mode of following instruction. 1) MVI BH,12H 2) ADD CL, [BX+04H]	02	CO3	R
v)	Write rules of Delay element method (at least 2)	02	CO4	U
vi)	List and explain any two characteristics of memory.	02	CO5	U
vii)	Perform addition of following floating point numbers. $(1010.11)_2 + (110.010)_2$	02	CO2	Ap
viii)	Consider, 5 stage pipeline architecture with 10 instructions. Draw Phase timing diagram and comment on Non-pipelined and Pipelined execution time.	02	CO6	U
Q.2	Solve any four questions out of six.	16		
i)	Differentiate Computer Architecture and Organization.	CO1	04	U
ii)	Represent $(14.125)_{10}$ in double precision floating point numbers.	CO2	04	Ap
iii)	Draw NAND based D flip flop.	CO3	04	U

iv)	Compare vertical and horizontal microprogramming.	CO4	04	U
v)	What is cache? List and Explain types of cache memory.	CO5	04	U
vi)	What are the types of Hazards in Pipeline? Explain any two with suitable examples.	CO6	04	U
Q.3	Solve any two questions out of three.	16		
i)	Draw and Explain the structural overview of a computer.	8	CO1	U
ii)	Explain Wilke's design for a microprogrammed control unit with a suitable diagram.	8	CO4	U
iii)	Consider a 2 way set associative memory mapping cache of size 4KB with block size of 256 bytes. The size of Main memory is 512 MB Find 1. No. of sets in main memory 2. No. of lines in cache. 3. No.of bits in tag 4. Represent physical address Show Memory mapping with the help of a suitable diagram. Also comments on the number of searches in 2 way set associative memory mapping.	8	CO5	Ap
Q.4	Solve any two questions out of three.	16		
i)	Perform 7 / 3 division using Non restoring division algorithm.	08	CO2	Ap
ii)	Draw and explain Instruction cycle state diagram with and without interrupt handling.	08	CO3	U
iii)	Describe Flynn classification in detail.	08	CO6	U

****