K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

April – May 2023

Program: B.Tech(Scheme: **II**)

Examination: **LY** Semester: **VIII**

Course Code: **EXDLC8023** Course Name: **System On Chip**

Date of Exam: **16/05/23** Duration: **2.5 Hours** Max. Marks: **60**

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		M	CO	BT
Q 1	Solve any six questions out of eight:	12		
i)	Draw a block diagram of a typical SOC showing the constituents blocks.	2	1	R
ii)	What are the architectural challenges in SOC system design?	2	2	U
iii)	What are the different types of assignment statements used inside always block in Verilog code?	2	3	A
iv)	What is self-checking testbench?	2	4	R
v)	Which is better compared to buffer and inverter? If so, Why?	2	5	U
vi)	How to Decide pin/pad location?	2	6	U
vii)	What is concurrency in SOC design?	2	2	U
viii)	a = 1'b1 b = 1'b0 y = {4{a,b}}. What will be the value of y for the above Verilog code?	2	3	A
Q.2	Solve any four questions out of six.	16		
i)	Explain the concepts 'Building a wrong chip' and 'Building a chip wrong'.	4	1	U
ii)	Compare early binding and late binding of interaction mechanism in terms of SOC designs.	4	2	U
iii)	Write a Verilog code for 4:1 mux synthesized to priority logic.	4	3	U
iv)	Write short note on emulators.	4	4	U
v)	Write short note on maze routing.	4	5	U
vi)	Write short note on power routing.	4	6	U
Q.3	Solve any two questions out of three.	16		
i)	Draw and explain detailed SOC design flow.	8	1	U
ii)	Write short note on RTL guidelines regarding following points a. FSM encoding	8	3	A

b. Combinational loops

iii)	Explain Clock Tree Synthesis in SOC design.	8	6	U
Q.4	Solve any two questions out of three.	16		
i)	What are the seven conditions that ensure balance among computation and communication?	8	2	U
ii)	Explain the top-down design and verification approach.	8	4	U
iii)	Explain floor planning in details.	8	5	U

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