27/05/2023

K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

May-June-2023

(B. Tech) Program: Electronics and Telecommunication
Examination: SY Semester: III

Course Code: EXC302 Course Name: Digital Logic Design
Duration: 2.5 Hours Max. Marks: 60

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	Convert $(532.125)_8$ into decimal, and binary.	02	CO1	U
ii)	Represent $(29)_{10}$ into Excess-3 code and Gray code	02	CO1	U
iii)	Give advantages of CMOS family	02	CO3	U
iv)	List VHDL operators	02	CO6	U
v)	Perform subtraction using 2's complement for $(10)_{10} - (7)_{10}$	02	CO2	U
vi)	Draw a JK flip-flop with a neat diagram and Truth table	02	CO4	U
vii)	State the difference between SRAM and DRAM	02	CO3	U
viii)	Compare the Combinational and Sequential Circuits.	02	CO5	U
Q.2	Solve any four questions out of six.	16		
i)	Implement full adder circuit using two 4:1 multiplexers	04	CO2	Ap
ii)	Write short note on ROM	04	CO3	U
iii)	State and prove the Demorgan's theorem.	04	CO2	U
iv)	Describe Priority Encoder & implement Logic Diagram for the same.	04	CO4	Ap

27/05/2023

v)	What is Programmable Array Logic(PAL)	04	CO5	Ap
vi)	Compare multiplexer and demultiplexer	04	CO2	U
Q.3	Solve any two questions out of three.	16		
i)	Design 3 to 8 line decoder with logic diagram and explain it.	08	CO2	Ap
ii)	Prove using Boolean algebra "NAND gate is an Universal Gate"	08	CO1	U
iii)	What is shift register? Explain working of serial in serial out. Give its applications	08	CO5	Ap
Q.4	Solve any two questions out of three.	16		
i)	Implement using only a) NAND gates b) NOR gates for f(0,1,2,3,8,9,12,13,14)	08	CO3	Ap
ii)	Design a 3-bit binary up/ down ripple counter. Draw the timing diagram.	08	CO4	Ap
iii)	Explain Modeling styles in VHDL	08	CO6	Ap

****