K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Subject Code: EXC 502 Subject Name: Digital VLSI Design Date:

B.Tech Program: **Electronics and Telecommunication**
Examination: **TY** Semester: **V**

Course Code: **EXC502** Course Name: **Digital VLSI Design**
Duration: **2.5 Hours** Max. Marks: **60**

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Write expression for the drain current of nMOS in saturation and linear region of operation.	2	1	R
ii)	Define propagation delay high to low (T_{PHL}) for COMS inverter.	2	2	R
iii)	Realize OR gate using Domino design style.	2	3	A
iv)	List different types of semiconductor memories.	2	4	R
v)	Draw Human Body Model (HBM) for Electrostatic Discharge (ESD).	2	5	R
vi)	List the steps involved in RTL design.	2	6	R
vii)	Draw 2:1 MUX using transmission gate.	2	3	A
viii)	List different colour codes used in stick diagram to represent different layers.	2	1	R
Q.2	**Solve any four questions out of six.**	**16**		
i)	Write a short note on scaling. Explain types of scaling.	4	1	U
ii)	Derive an expression for input low voltage (V_{IL}) of CMOS inverter.	4	2	U
iii)	Explain CMOS latch-up problem in static CMOS design style.	4	3	U
iv)	Design a NAND ROM to save the given binary data: 0100, 1001, 1000, 1010	4	4	A
v)	Demonstrate addition of $(1101\ 1000\ 0101\ 1110)_2$ and $(0011\ 1001\ 0010\ 0001)_2$ using Carry Select Adder.	4	5	A
vi)	Draw a datapath for 3 tap FIR filter using RTL design.	4	6	A

Q.3	**Solve any two questions out of three.**	**16**		
i)	Draw stick diagram and mask layout for CMOS NOR gate.	8	1	A
ii)	Draw 3T-DRAM cell. Explain read '0', write '0', read '1' and write '1' operation.	8	4	U
iii)	Design Soda Dispenser machine using RTL design.	8	6	C
Q.4	**Solve any two questions out of three.**	**16**		
i)	Consider a CMOS inverter with the following parameters: nMOS : Vt,n = 0.48 V μnCox= 102 μA/V2 (W/L)n= 10 pMOS : Vt,p = -0.46 V μpCox= 51.6 μA/V2 (W/L)p= 19 Calculate the noise margin high. The power supply voltage is VDD = 1.2 V.	8	2	A
ii)	Design static CMOS circuit for full adder using mirror circuit.	8	3	A
iii)	Draw 4 bit array multiplier. Highlight the worst case delay path. Find out the worst case delay if propagation delay of the components is as follows: AND gate: 1ns Half Adder: 2ns Full Adder: 2ns	8	5	A

****