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K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

April – May 2023
(B.Tech.) Program: AI & DS Scheme I/II: I
Examination: SY Semester: IV
Course Code: IUAIC405 Course Name: Microprocessor
Date of Exam: 03/06/2023 Duration: 3 Hours Max. Marks: 60

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	Discuss the instruction Que in the BIU of 8086	2	1	U
ii)	What is ISR? Explain its structure in brief using suitable example	2	2	U
iii)	What is a Macro. Explain in brief with a suitable example	2	3	R
iv)	List formats of I/O mode Control Words for PPI 8255	2	3	U
v)	List bit manipulation instructions in 8086	2	4	U
vi)	What is the use of L1 cache in Pentium	2	5	U
vii)	What is memory banking in 8086	2	5	A
viii)	What are the typical clock speeds for Pentium microprocessors	2	6	R
Q.2	Solve any four questions out of six.	16		
i)	Compare minimum mode and maximum mode of operation in microprocessor 8086	4	1	U
ii)	Discuss JUMP commands with suitable examples	4	2	U
iii)	Explain DMA data transfer modes in DMAC 8259	4	3	U
iv)	Explain how physical address is calculated in 8086	4	1	U
v)	What are the advantages and disadvantages of using memory-mapped I/O compared to port-mapped I/O?	4	5	U
vi)	Discuss DMA controller for 8086	4	4	U

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Q.3	Solve any two questions out of three.	16		
i)	Explain architecture of microprocessor 8086	8	1	U
ii)	Discuss addressing modes of 8086 with suitable examples.	8	2	U
iii)	Discuss use of interrupts for 8086	8	3	U
Q.4	Solve any two questions out of three.	16		
i)	Discuss the use of PIC with 8086	8	4	U
ii)	Discuss minimum mode of operation of 8086	8	1	U
iii)	What is the superscalar architecture of the Pentium microprocessor, and how does it differ from the previous generations of x86 processors? How does the Pentium achieve higher performance through its use of parallel execution?	8	6	U
