K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Nov/Dec 2023

B.Tech Program: **Electronics and Telecommunication** Scheme: **II**
Examination: **TY** Semester: **V**
Course Code: **EXC502** Course Name: **Digital VLSI Design**
Date of Exam: **30/11/23** Duration: **2.5 Hours** Max. Marks: **60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Draw symbols for nMOS and pMOS, showing all four terminals.		1	R
ii)	Define propagation delay low to high.		2	R
iii)	Write advantages of static CMOS design style.		3	U
iv)	Differentiate between NOR based ROM and NAND based ROM.		4	U
v)	Draw a block diagram of 4-bit Ripple Carry Adder.		5	R
vi)	Differentiate between HLSM and FSM.		6	U
vii)	Realize following expression using static CMOS design style. y = /(A+BC)		3	A
viii)	Draw output VI characteristics of nMOS.		1	R
Q.2	**Solve any four questions out of six.**	**16**		
i)	What are different components of channel capacitance in a MOSFET? Write expression for all channel capacitance components in different mode of operations.		1	U
ii)	Draw and explain voltage transfer characteristics of CMOS inverter.		2	U
iii)	Realize 8:1 Mux using Transmission Gate.		3	A
iv)	Write short note on flash memory.		4	U
v)	Name and draw different Electrostatic Discharge Models.		5	U
vi)	Design LASER based distance measurer using RTL design technique.		6	C
Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain the steps in the fabrication of nMOS with neat diagram.		1	U
ii)	Realize JK latch using static CMOS design style.		3	A
iii)	Draw and explain addition of 7 multi-bit operands using Carry Save Adder.		5	U

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Q.4 Solve any two questions out of three. **16**

i)	Calculate fall time for a CMOS inverter using average current method, if V_{DD}= 5V, $\mu_n C_{OX} = 20\mu A/V^2$, $\mu_p C_{OX} = 12\mu A/V^2$, $(W/L)_n = 10$, $(W/L)_p = 15$, $V_{t,n} = 1$ V, $V_{t,p} = -1$ V and load capacitance is 1pF.	2	A
ii)	Design a NAND based ROM to store 0011, 1001, 0100 and 1110. Explain its operation to read different data. Also draw stick diagram for the same.	4	A
iii)	Design a 3 tap FIR filter using RTL design technique. Also calculate the critical delay if the delay of an adder is 2ns and multiplier is 20ns.	6	C

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