K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Supplementary Exam
August 2023
B. Tech: Electronics and Telecommunication

Examination: SY
Course Code:EXC402
Duration: 2.5 Hours

Semester: IV
Course Name: Microcontrollers
Date : 25/08/2023

Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

Q. No.	Question	Max. Marks	CO	BT Level
Q 1	**Solve any six questions out of eight:**	12		
i)	Distinguish between VON- NEUMANN & HARVARD CPU Architecture.	2	1	U
ii)	List the important features of 8051 microcontrollers.	2	1	U
iii)	Discuss Instruction Syntax wrt ARM-7	2	5	U
iv)	Compare between SJMP , LJMP and AJMP instructions.	2	4	U
v)	List 8051 Data types and directives	2	3	U
vi)	Distinguish between Thumb state and ARM state.	2	6	U
vii)	Discuss the semiconductor memories	2	2	U
viii)	List any five bit addressable SFRs in 8051 with their physical address.	2	4	U
Q.2	**Solve any four questions out of six.**	16		
i)	Classify Memory : Primary and Secondary	4	2	U
ii)	What are the sources of interrupt in 8051? List them with their priority and vector addresses.	4	1	U

iii)	Explain Addressing modes in 8051	4	4	U
iv)	Compare Call and Jmp instructions	4	3	U
v)	Explain ARM 7 CPSR and SPSR	4	5	U
vi)	Explain the concept of CORTEX A, CORTEX R and CORTEX M with respect to ARM.	4	6	U
Q.3	**Solve any two questions out of three.**	16		
i)	What is stack and stack pointer, explain stack in 8051	8	1	U
ii)	Explain Operating Modes of ARM-7 in Details	8	5	U
iii)	Explain Serial communication in 8051	8	3	U
Q.4	**Solve any two questions out of three.**	16		
i)	Explain Virtual Memory Concept with Memory Management	8	2	Ap
ii)	Draw and explain internal RAM organisation in 8051.	8	4	U
iii)	What is load store architecture in ARM processors? With respect to ARM programmer's model, explain various general purpose and special purpose registers in ARM 7.	8	6	U