K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Supplementary Examination of August 2023
(B. Tech) Program: Electronics and Telecommunication Engineering
Scheme II
Examination: SY Semester: IV
Course Code: **EXC403** and Course Name: **Linear Integrated Circuit**

| Date of Exam: 28/08/2023 | Duration: 2.5 Hours | Max. Marks: 60 |

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	12		
i)	Draw circuit of non-inverting amplifier; also mention its gain formula.	2	1	U
ii)	Explain free running state in PLL.	2	6	U
iii)	Explain the Function of threshold Pin in IC555.	2	4	R
iv)	Define rectifiers? State its advantages precision rectifier over normal rectifier.	2	3	U
v)	What is monostable multivibrator? List its applications.	2	4	R
vi)	Draw the circuit diagram of RC phase shift oscillator and mention its frequency and β formula.	2	3	R
vii)	What is a window detector? Draw the circuit diagram of window detector.	2	4	U
viii)	Write features of IC 723.	2	5	U
Q.2	**Solve any four questions out of six.**	16		
i)	Draw and explain PLL as FSK demodulator.	4	6	U
ii)	Realize a circuit for $Vo = (-4V_1 - 2V_2 + 3V_3)$ using opamp and resistors.	4	1	A
iii)	Describe the circuit operations of the following V-I converters, Grounded load V–I convertor.	4	2	U

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iv)	With a neat circuit diagram. Explain the working of the inverting comparator circuit.	4	3	U
V)	Write a short note on the pulse position modulator using IC 555.	4	4	R
Vi)	Draw Pin of IC 723.	4	5	U
Q.3	**Solve any two questions out of three.**	16		
i)	Design an Astable multivibrator using 555 timers for a frequency of 1KHz and a duty cycle of 70 %. Assume c=0.1µf	8	4	A
ii)	Draw and explain the functional diagram of the IC723 voltage regulator.	8	5	U
iii)	Derive an expression for subtractor as op –amp and also Design a circuit to perform the difference between two signals V1 & V2 which is to be amplified by factor of 10.	8	1	R
Q.4	**Solve any two questions out of three.**	16		
i)	Design 2nd order LPF for cut off frequency of 1 KHZ and pass band gain of 1.586.	8	2	A
ii)	Design a practical integrator to operate at f = 4KHZ and gain is equal to 2.	8	3	A
iii)	Draw a neat circuit diagram of an instrumentation amplifier using 3 op amps. Derive the expression for its gain. How can its gain be varied? What are its advantages over a difference amplifier using single op-amp	8	6	U

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