K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Supplementary Exam Feb/Mar 2024

B.Tech Program: **Electronics and Telecommunication** Scheme: **II**
Examination: **TY** Semester: **V**
Course Code: **EXC502** Course Name: **Digital VLSI Design**
Date of Exam: 29-02-2024 Duration: **2.5 Hours** Max. Marks: **60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Draw a capacitance model for an nMOS.		1	R
ii)	Define rise time for CMOS inverter.		2	R
iii)	Realize OR gate using Transmission gate.		3	A
iv)	What are different types of semiconductor memory?		4	R
v)	Write expression for propagate and generate signal in Carry Look Ahead Adder.		5	R
vi)	Write down the steps involved in RTL design.		6	R
vii)	Realize two input NOR gate using C^2MOS design style.		3	A
viii)	Write expression for drain current for nMOS in linear region. Also write meaning of all terms.		1	U
Q.2	**Solve any four questions out of six.**	**16**		
i)	Draw and explain VI characteristics of nMOS.		1	U
ii)	Draw an equivalent CMOS inverter for y = /(A+BC) realized using static CMOS. (W/L) ratio for all pMOS is 12 and 8 for all nMOS.		2	A
iii)	Explain the problem of charge leakage in dynamic CMOS.		3	U
iv)	Design a NOR based ROM to store 1001, 0101, 0010, 1100.		4	A
v)	Demonstrate addition of $(1010\ 0101\ 1001\ 0010)_2$ and $(0101\ 0010\ 0111\ 0100)_2$ using Carry Select Adder.		5	A
vi)	Design 3 tap FIR filter using RTL design technique.		6	C
Q.3	**Solve any two questions out of three.**	**16**		
i)	Draw stick diagram and mask layout for CMOS inverter adhering to lambda rules.		1	A
ii)	Derive an expression for V_{OH} and V_{IH} of a CMOS inverter.		2	U

iii)	Design Soda Dispenser Machine using RTL design technique.	6	C

Q.4 Solve any two questions out of three. **16**

i)	Realize y = /(AB+CD) using following design styles, a) Static CMOS b) Dynamic CMOS c) Pseudo nMOS	3	A
ii)	Draw 1-T DRAM cell. Explain precharge, read and refresh operation.	4	U
iii)	Draw 4-bit array multiplier. Calculate the maximum path delay if the propagation delay for an AND gate is 2ns and adder is 4ns.	5	An

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