DECEMBER- 2019

EXAMINATION TIME TABLE
PROGRAMME - S.E. (Electronics) (REV. -2012)(CBSGS)
SEMESTER – IV

Days and Dates	Time	Paper Code	Paper
Wednesday, December 04, 2019	02:30 p.m. to 05:30 p.m.	39301	DISCRETE ELECTRONIC CIRCUITS
Monday, December 09, 2019	02:30 p.m. to 05:30 p.m.	39302	APPLIED MATHEMATICS - IV
Wednesday, December 11, 2019	02:30 p.m. to 05:30 p.m.	39303	MICROPROCESSOR AND PERIPHERALS
Friday, December 13, 2019	02:30 p.m. to 05:30 p.m.	39304	PRINCIPLES OF CONTROL SYSTEMS
Tuesday, December 17, 2019	02:30 p.m. to 05:30 p.m.	39305	FUNDAMENTALS OF COMMUNATION ENGINEERING
Thursday, December 19, 2019	02:30 p.m. to 05:30 p.m.	39306	ELECTRICAL MACHINES

(Dr. Vinod Patil

(Three Hours) **(80 Marks)**

N.B. 1**) Question-1** is compulsory and solve any **Three** questions from remaining questions
2)Assume suitable data if it is required

Que-1	Answer any **FIVE**		
a	Explain any one Clamping circuit with proper waveforms.		4
b	Explain any one biasing method of JFET circuit with proper circuit diagram.		4
c	What are the advantages of Multistage amplifier?		4
d	Classify oscillator circuits with reference to frequency.		4
e	What are different techniques to improve CMRR in differential amplifier, explain any one.		4
f	How Power amplifier is different than Voltage Amplifier.		4
Que-2a	For the Voltage divider biased circuit using BJT with the following data $R_1 = 39\ K\Omega$, $R_2 = 3.9\ K\Omega$, $R_C = 10\ K\Omega$, $R_E = 1.5\ K\Omega$, $C_1 = C_2 = C_E = 10\ \mu F$, $\beta = 140$, $V_{BE} = 0.7\ V$, $V_{CC} = 22\ V$ Determine V_{CEq}, I_{Cq} and state in which region the circuit is working.		10
b	Derive equation of Av, Ri and Ro for Voltage Divider biased JFET amplifier circuit.		10
Que-3a	Draw two stage CE-CE amplifier circuit, hence draw its ac equivalent model and derive ac parameters for each stage.		10
b	Draw Block diagrams of different types of negative feedback amplifiers.		10
Que-4a	For BJT differential amplifier derive equations of A_{DM}, A_{CM} and CMRR.		10
b	Compare E-Mosfet and D-Mosfet Amplifier		10
Que-5a	Explain Class B Power Amplifier in brief.		10
b	Explain Low frequency response of JFET amplifier.		10
Que-6	Write short Notes on **any FOUR** of the following:		20
a	Condition of Sustained Oscillations in Oscillator		
b	Wilson Current Source		
c	Types of Power Amplifiers		
d	DC load line of BJT circuit		
e	Clipping Circuit		

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(3 Hours) **(Total Marks : 80)**

N.B.: 1) **Question No. 1** is **Compulsory**.
2) Attempt **any three** from the **remaining**.

1. a) Find the extremal of $\int_{x_0}^{x_1} \frac{1+y^2}{y'^2} dx$. **(05)**

b) Is the following set of vectors in P_2 linearly independent? $2-x+4x^2$, $3+6x+2x^2$, $2+10x-4x^2$? **(05)**

c) Show that Eigen values of Hermitian matrix are real. **(05)**

d) Evaluate $\int(z^2-2\bar{z}+1)\,dz$ over a closed circle $x^2+y^2=2$. **(05)**

2. a) Find the extremal $\int_0^{\pi}(y^2-y'^2-2ycosx)dx,\quad y(0)=0,\ y(\pi/2)=0$. **(06)**

b) Find the Eigen Values and Eigen Vectors of the matrix A^3+3I, where **(06)**

$$A=\begin{bmatrix}2 & -2 & 3\\ 1 & 1 & 1\\ 1 & 3 & -1\end{bmatrix}$$

c) Obtain all possible expansion of $f(z)=\frac{z}{(z-1)(z-2)}$ about $z=-2$ indicating region of convergence. **(08)**

3. a) Verify Cayley - Hamilton Theorem for $A=\begin{bmatrix}1 & -1 & 0\\ 2 & 3 & -2\\ -2 & 0 & 1\end{bmatrix}$ and find A^{-1}. **(06)**

b) Using Cauchy's Residue Theorem evaluate $\int_C \frac{e^z}{z^2+\pi^2} dz$ where C is |z|=4. **(06)**

c) Show that a closed curve 'C' of a given fixed length (perimeter) which encloses maximum area is a circle. **(08)**

4. a) Find an orthonormal basis for the subspace of R^3 by applying Gram-Schmidt process, where $u_1=(1,0,1,1), u_2=(-1,0,1,1), u_3=(0,-1,1,1)$. **(06)**

b) Find A^{20} for the matrix $A=\begin{bmatrix}2 & 3\\ -3 & -4\end{bmatrix}$. **(06)**

c) Reduce the Quadratic Form $2xy+2yz+2zx$ to diagonal form by orthogonal reduction method. **(08)**

5. a) Using Rayleigh-Ritz Method, find an approximate solution to the extremal problem $\int_0^1(y'^2-y^2-2yx)dx,\quad y(0)=0,\ y(1)=0$. **(06)**

b) Let V be a vector space containing 2×2 matrices and $W\subseteq V$ such that $W=\begin{bmatrix}a & 0\\ 0 & b\end{bmatrix}$. Is W a subspace of V? Justify. **(06)**

c) Show that the matrix $A=\begin{bmatrix}8 & -8 & -2\\ 4 & -3 & -2\\ 3 & -4 & 1\end{bmatrix}$ is diogonable.Also find the transforming matrix and diagonal matrix. **(08)**

6. a) Using Cauchy's Residue Theorem, evaluate $\int_0^{2\pi}\frac{d\theta}{13+5\,sin\theta}$. **(06)**

b) Evaluate $\int_{1-i}^{2+i}(2x+1+iy)dz$ along the curve $x=t+1, y=2t^2-1$. **(06)**

c) Find the singular value decomposition of the matrix A= $\begin{bmatrix}2 & 3\\ 0 & 2\end{bmatrix}$ **(08)**

Q.P. Code :24107

Total Marks: 80 **(3 Hours)**

Note: 1. Question No. 1 is compulsory.

2. Solve any three from the remaining five questions.

3. All questions carry equal marks.

1.a. Explain the significance of Logical address and physical address in the 8086. (05)

b. Explain any four addressing modes of the 8086 with a neat example of each. (05)

c. Explain the function of the bits in the I/O control word of the 8255 PPI. (05)

d. Explain the function of the queue in the 8086. (05)

2.a. Write an assembly language program for the 8086 to transfer a block of data from one memory location to the other (Use string instructions). (10)

b. What is bus arbitration? Explain the role of the bus arbiter like 8289 in bus arbitration. (10)

3.a. What is Memory segmentation? Explain in detail the advantages of Memory segmentation. (10)

b. Draw an interfacing diagram of the 8086 and the 8255 PPI and explain the signals. (10)

4.a. Explain the sequence of events that take place in case of an interrupt occurrence in the 8086. Also, explain the significance of the interrupt vector table (IVT). (10)

b. Interface 16kB of ROM and 16KB of RAM to the 8086. Show the address decoding. (10)

5.a. Explain the 8086-8087 interface with a neat diagram. Also , mention the function of each of the interfacing signals. (10)

b. Explain the following w.r.t 8259 PIC : (10)

i. ICW1

ii. AEOI

iii. SFNM mode

iv. OCW3

6. Write short notes on: (20)

a. Programmer's model of the 8085

b. 8237 DMA Controller

c. 8284 clock generator

(3 hours) **[Marks:80]**

NOTE: 1) Question No. 1 is compulsory.
2) Out of remaining questions, attempt any 3 questions.
3) In all 4 questions to be attempted.
4) All questions carry equal marks.
5) Figures in brackets on the right hand side indicate full marks.
6) Assume Suitable data if necessary

Q1 Answer any 5

i) How do you compare open loop and closed loop system? 4
ii) What are position, velocity and acceleration error coefficients? 4
iii) What is importance of state space representation? 4
iv) Write expression for rise time, peak time, maximum peak overshoot and settling time of second order under damped system. 4
v) How to find breakaway point in root locus 4
vi) How do you define stable system? 4
vii) What are properties of state transition matrix? 4

Q2a) Check whether the following systems are stable using Routh's stability criterion 10

i) $3s^4+10s^3+5s^2+2$

ii) $s^4+4s^3+6s^2+4s-5$

2b) Find root locus for the transfer function $G(s)=\frac{2}{s(s+2)(s+5)}$ 10

3a) Find the state equation and output equation for the transfer function 10

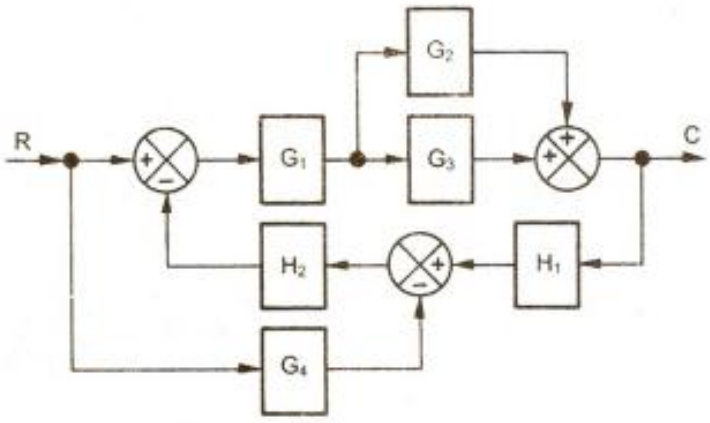
$$G(s)=\frac{2s+1}{s^2+7s+9}$$

3b) Check the controllability and observability of the following system 10

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\\ \dot{x}_3\end{bmatrix}=\begin{bmatrix}0 & 1 & 0\\ 0 & 0 & 1\\ -1 & -2 & -3\end{bmatrix}\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}+\begin{bmatrix}0\\ 0\\ 1\end{bmatrix}u$$

$$y=[0 \quad 0 \quad 1]*\begin{bmatrix}x_1\\ x_2\\ x_3\end{bmatrix}$$

4a) Reduce the following Block diagram using Block reduction technique 10



4b) Draw Bode plot for the function $G(s) = \frac{40(s+2)}{s(s+10)(s+400)}$ and find gain margin and phase margin 10

5a) Explain signal flow graph representation and its reduction technique using Masons gain formula 10

5b) Draw polar plots for 10

$i) \frac{1}{s+10}$

$ii) \frac{1}{s^2}$

$iii) \frac{100}{s^3}$

$iv) \frac{10}{s}$

6. Write short notes on any 4 20
   i. Nyquist plots
   ii. Lead and lag compensator
   iii. Correlation between time and frequency response
   iv. Gain and phase margin
   v. Type and order of system

(3 Hours) **[Total Marks: 80]**

1) Question 1 is compulsory
2) Solve any three from the remaining five questions
3) Assume suitable data if necessary.
4) Figures to the right indicate full marks

Q.1. Answer any **four questions** from the following: [20]

a What are pre emphasis and De emphasis circuits?

b What is vestigial sideband transmission? Where is it used?

c Discuss the need for modulation in wireless communication system.

d Why is PCM more resistant to noise?

e Explain the significance of noise figure.

Q.2.a Why the local oscillator frequency is always kept higher than the incoming signal frequency in a super heterodyne receiver? [05]

b. For an AM DSBFC wave with a carrier power of 5 W and a modulation coefficient of 1, determine the upper and lower sideband powers and the total modulated power. [05]

c. What is the importance of proper choice of RC time constant in an AM detector circuit? Explain with neat diagrams the distortions caused by improper time constant. [10]

Q.3.a With the help of a neat circuit diagram, explain the working of Foster Seeley discriminator. What is its disadvantage? [10]

b. Discuss the shortcomings of TRF receiver. [05]

c. Why is AGC needed in super heterodyne receivers? [05]

Q.4.a Justify the statement: "Multiplexing helps in proper use of communication resources" [10]

b. Discuss in detail any two sampling techniques. [10]

Q.5.a. Explain the term companding as applied to Pulse Code Modulation. Why is Delta modulation an extreme case of PCM? [10]

b. For a sinusoidal modulating signal, draw PPM, and PWM pulses. [05]

c. Discuss a simple method of noise suppression in an FM wave. [05]

Q.6 Write short notes on **any four**: [20]

a) Choice of intermediate frequency in a super heterodyne receiver
b) Sky wave propagation
c) Delta modulation
d) Varactor diode detector
e) Image frequency

[Time: 3 Hours] **[Marks:60]**

Please check whether you have got the right question paper.

N.B:
1. **Question.No.1** is **compulsory**.
2. Attempt any **three** questions from remaining **five** questions.
3. **Figures** to **right** indicate **full marks**.
4. Assume suitable **data**, if **any**.

Q 1

(a)	Explain the necessity of starter in D.C. Motor	**05**
(b)	State the important applications of brushless DC motor	**05**
(c)	A 4 pole, 50 Hz induction motor has full load speed of 1440 rpm. Calculate slip.	**05**

Q2

(a)	Explain construction and working principle of 3 phase squirrel cage induction motor.	**08**
(b)	What are the advantages, disadvantages and applications of switched reluctance motor?	**07**

Q3

(a)	Explain the principle of operation of capacitor start and capacitor run single phase induction motor.	**08**
(b)	Describe the construction and working principal of variable reluctance motor.	**07**

Q4

(a)	State the different types of brushless dc motor and explain any one.	**07**
(b)	Explain different speed control methods of DC shunt motor	**08**

Q5

(a)	Compare the different starting methods of three phase induction motor	**07**
(b)	Explain with neat sketches the armature reaction in DC machine	**08**

Q6 Write short notes on any three

(a)	The double field revolving theory in single phase induction motor	**05**
(b)	Permanent magnet synchronous motor.	**05**
(c)	Drive circuit of stepper motor	**05**
(d)	Control requirement for switched reluctance motor	**05**
