

**K. J. SOMAIYA INSTITUTE OF MANAGEMENT STUDIES AND RESEARCH**  
**MCA SEM- I End Term Examination November 2016**

**Subject: - Computer Organization and Architecture**

**Maximum Marks: 50**

**Duration: 3 hrs**

**25/11/2016**

**Note: Q1 is Compulsory.**

**Solve any 4 from Questions 2 to 7.**

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|---------------|--|----------|
| <b>Q1. a.</b> | <b>Explain the functions of multiplexer and demultiplexer. Draw logic circuit for 8 to 3 multiplexer and 3 to 8 demultiplexer.</b> | <b>5</b> |
| <b>b.</b>     | <b>Explain the instruction cycle with indirect addressing.</b>   | <b>5</b> |
| <b>Q2. a.</b> | <b>Simplify using K-map <math>F(A,B,C,D)=\Sigma(0,1,3,4,5,7,10,11)</math></b>  | <b>5</b> |
| <b>b.</b>     | <b>Simplify the following Boolean expressions. Write the rules used in each step of simplification.</b>                            | <b>5</b> |
| <b>a)</b>     | <b><math>Q = B.(A + \bar{C}) + A + A.(\bar{A} + B)</math></b>  |          |
| <b>b)</b>     | <b><math>Q = AB.(\bar{B} + C) + BC + B</math></b>  |          |
| <b>Q3. a.</b> | <b>Describe the execution of multiple interrupts with suitable example.</b>  | <b>5</b> |
| <b>b.</b>     | <b>Explain programmed and interrupt driven I/O techniques with flow diagram.</b>   | <b>5</b> |
| <b>Q4. a.</b> | <b>Differentiate between SRAM and DRAM.</b>  | <b>5</b> |
| <b>b.</b>     | <b>Describe cache read operation with flow diagram.</b>  | <b>5</b> |
| <b>Q5. a.</b> | <b>Explain different shift and rotate operations in instruction set.</b>   | <b>5</b> |
| <b>b.</b>     | <b>Describe register and register indirect addressing modes.</b>   | <b>5</b> |
| <b>Q6. a.</b> | <b>How branching is handled in instruction pipelining.</b>   | <b>5</b> |
| <b>b.</b>     | <b>Explain different superscalar instruction issue policies.</b>   | <b>5</b> |
| <b>Q7. a.</b> | <b>Write notes on micro programmed and hardwired control unit.</b>   | <b>5</b> |
| <b>b.</b>     | <b>Explain symmetric multiprocessor architecture.</b>  | <b>5</b> |

*All the Best!!!*