# University of Mumbai
## Examination 2020 under Cluster 06
## (Lead College :- Vidyavardhini's College of Engineering & Technology)

**Examinations Commencing from 7th January 2021 to 20th January 2021**

Program: **Electronics Engineering**

Curriculum Scheme: Rev. 2019

Examination: S.E. Semester III

Course Code: ELC302 and Course Name: Electronic Devices & Circuits – I

Time: 2 hour | Max. Marks: 80

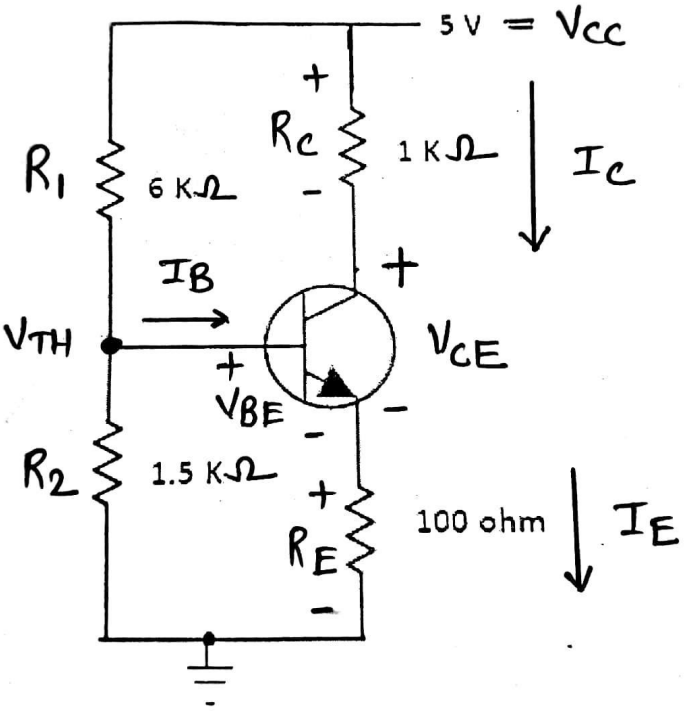
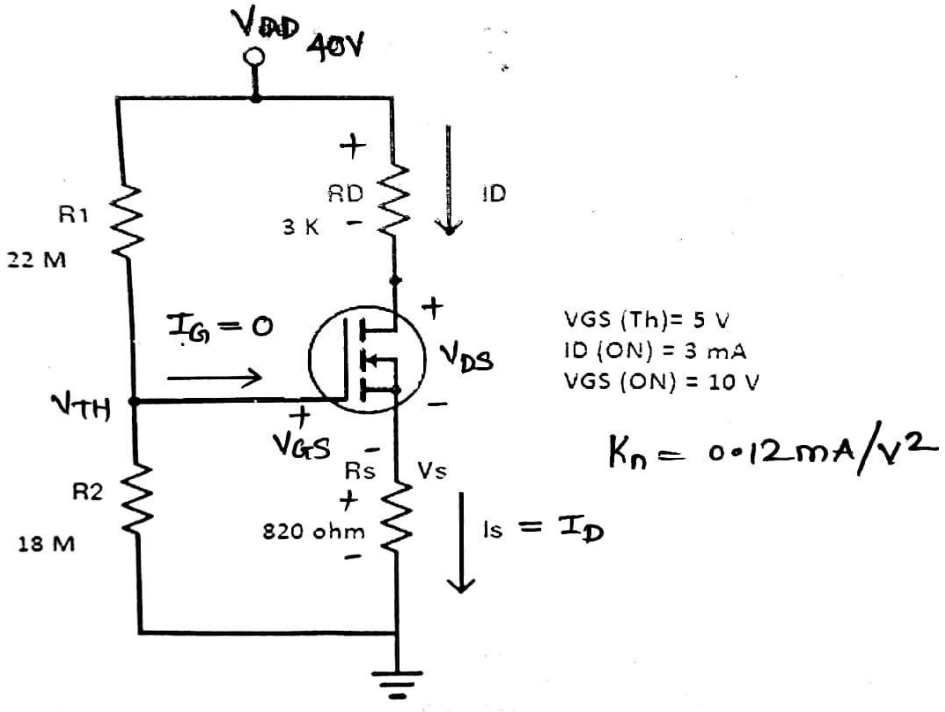
---

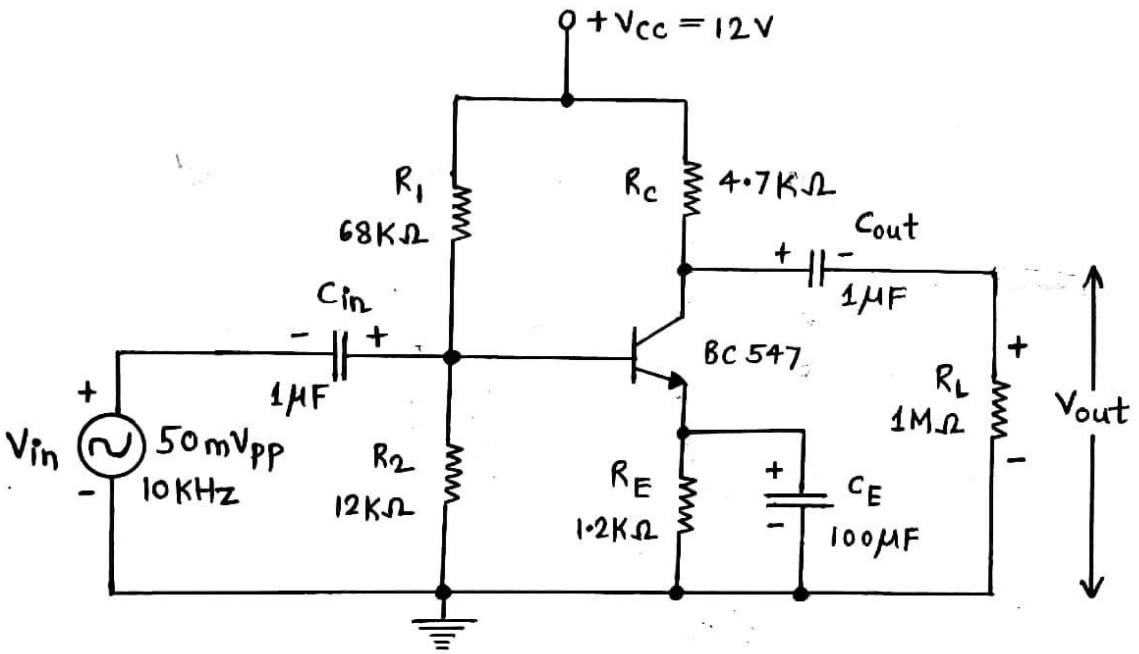
| **Q.1** | **Choose the correct option for following questions. All the Questions are compulsory and carry equal marks.** |
|---|---|
| 1. | The capacitance in a reverse biased PN junction is called as :- |
| Option A: | Terminal capacitance |
| Option B: | Junction capacitance |
| Option C: | Diffusion capacitance |
| Option D: | Transition capacitance |
| | |
| 2. | In any semiconductor material, the diffusion current is proportional to :- |
| Option A: | Applied electric field |
| Option B: | Concentration gradient of charge carriers |
| Option C: | Square of applied electric field |
| Option D: | Cube of applied electric field |
| | |
| 3. | The phenomenon of Zener breakdown occurs in :- |
| Option A: | Heavily doped PN junction |
| Option B: | Lightly doped PN junction |
| Option C: | Moderately doped PN junction |
| Option D: | Forward biased PN junction |
| | |
| 4. | Forward break-over voltage ($V_{FBO}$) of a typical silicon diode is approximately :- |
| Option A: | 0.6 V – 0.7 V |
| Option B: | 0.2 V – 0.3 V |
| Option C: | 1.1 V – 1.2 V |
| Option D: | 0.1 V – 0.2 V |
| | |
| 5. | When a reverse current in Zener diode increases from 20 mA to 30 mA, Zener voltage changes from 5.6 V to 5.65 V. The Zener resistance ($r_z$) is given by :- |
| Option A: | 2 Ω |
| Option B: | 3 Ω |
| Option C: | 4 Ω |
| Option D: | 5 Ω |
| | |
| 6. | In bipolar junction transistor (BJT) which mode of operation is not commonly used in real life applications ? |
| Option A: | The inverse / reverse mode of operation |
| Option B: | The cut-off mode of operation |
| Option C: | The saturation mode of operation |
| Option D: | The forward active / linear mode of operation |

| | |
|---|---|
| | |
| 7. | In bipolar junction transistor (BJT) the Early effect is due to :- |
| Option A: | Decrease in width of the emitter due to reverse bias of collector-to-base junction |
| Option B: | Decrease in width of the base due to reverse bias of collector-to-base junction |
| Option C: | Decrease in width of collector due to reverse bias of collector-to-base junction |
| Option D: | Temperature variations resulting in thermally generated minority carriers |
| | |
| 8. | In PNP bipolar junction transistor (BJT), stream of current in active region is due to :- |
| Option A: | Drift of holes |
| Option B: | Drift of electrons |
| Option C: | Diffusion of holes |
| Option D: | Diffusion of electrons |
| | |
| 9. | In a bipolar junction transistor (BJT) if $\beta = 100$ & collector current ($I_C$) is 30 mA then what is the value of base current ($I_B$) ? |
| Option A: | 0.03 mA |
| Option B: | 0.3 mA |
| Option C: | 3 mA |
| Option D: | 300 mA |
| | |
| 10. | The field effect transistor (FET) is :- |
| Option A: | Power controlled device |
| Option B: | Energy controlled device |
| Option C: | Current controlled device |
| Option D: | Voltage controlled device |
| | |
| 11. | Pinch-off voltage in field effect transistor (FET) is :- |
| Option A: | Drain-to-source voltage giving zero (no) drain-to-source current |
| Option B: | Drain-to-source voltage giving maximum drain-to-source current |
| Option C: | Gate-to-source voltage giving zero (no) drain-to-source current |
| Option D: | Gate-to-source voltage giving maximum drain-to-source current |
| | |
| 12. | Which of the following statement is not true for any field effect transistor (FET) ? |
| Option A: | FET has very high input resistance / impedance as compared to BJT |
| Option B: | FET is a majority carrier operated (unipolar) device |
| Option C: | FET has excellent operating stability against temperature variations compared to BJT |
| Option D: | FET has higher transconductance compared to BJT |
| | |
| 13. | In junction field effect transistor (JFET), the amplification factor ($\mu$) is expressed by which of the following mathematical expressions ? |
| Option A: | $\mu = g_m \times r_d$ |
| Option B: | $\mu = g_m + r_d$ |
| Option C: | $\mu = g_m - r_d$ |
| Option D: | $\mu = g_m / r_d$ |
| | |
| 14. | For metal oxide semiconductor field effect transistor (MOSFET), the input impedance or the input resistance ($R_i$ or $Z_i$) is :- |
| Option A: | Less than JFET but more than BJT |
| Option B: | More than both, JFET & BJT |
| Option C: | More than JFET but less than BJT |
| Option D: | Less than both, JFET & BJT |

| | |
|---|---|
| | |
| 15. | In MOSFET, which terminal is electrically isolated from the entire device structure ? |
| Option A: | Source (S) |
| Option B: | Drain (D) |
| Option C: | Gate (G) |
| Option D: | Bulk or Body or Substrate (SS) |
| | |
| 16. | In design of filters, which of these has the lowest value of ripple factor (γ) ? |
| Option A: | Capacitor (C) Filter |
| Option B: | Inductor (L) Filter |
| Option C: | Inductor & Capacitor (L-C) Filter |
| Option D: | C-L-C or 'π' Filter |
| | |
| 17. | Maximum operating efficiency of a full wave bridge type rectifier to be considered during the design process is :- |
| Option A: | 25 % |
| Option B: | 40.6 % |
| Option C: | 81.2 % |
| Option D: | 50 % |
| | |
| 18. | Which of these statements in not true for any type of BJT common base (CB) configuration amplifier ? |
| Option A: | It has a low input impedance / resistance |
| Option B: | It has a high output impedance / resistance |
| Option C: | It has moderate to high voltage gain |
| Option D: | It produces a phase shift in amplified output signal with respect to input signal applied |
| | |
| 19. | Which process of electron-hole pair (EHP) is responsible for emitting of light ? |
| Option A: | Recombination |
| Option B: | Diffusion |
| Option C: | Breakdown |
| Option D: | Ionization |
| | |
| 20. | Which of these diodes does not work in the reverse bias mode of operation ? |
| Option A: | Light emitting diode (LED) |
| Option B: | Zener diode |
| Option C: | Varactor diode |
| Option D: | Photo diode |

| **Q.2 (20 Marks)** | **Solve any Four out of Six** **05 Marks Each** |
|---|---|
| A | Explain the effects of temperature on the V – I characteristics of PN junction diode with a neat sketch / diagram & appropriate mathematical expressions. |
| B | Describe forward bias V – I characteristics of PN junction diode with neat labeled diagram & appropriate sketch. |
| C | Explain working of Center Tap type full wave rectifier with help of circuit diagram. |
| D | Discuss the working / operation of dual end clipper circuit with a neat labeled diagram showing appropriate waveforms of the resulting clipped output voltage. |
| E | Explain the operation of Zener diode as a voltage regulator with a neat sketch for condition where supply / source voltage remains constant but load resistor varies. |

| | |
|---|---|
| F | With a neat sketch, describe the operating principle & the construction of the light emitting diode (LED). |
| **Q.3 (20 Marks)** | **Solve any Two out of Three** **10 Marks Each** |
| A | For a voltage divider bias circuit shown in Fig. 1 using Silicon (Si) BJT with β = 100 calculate the Q – point where Q = [$V_{CE}$, $I_C$].   **Fig. 1 for Q.3 (A)** |
| B | For the voltage divider bias circuit shown in Fig. 2 using N-channel E-MOSFET calculate Q – point where Q = [$V_{DS}$, $I_D$].   |

| | |
|---|---|
| | **Fig. 2 for Q.3 (B)** |
| C | Fig. 3 shows a single stage CE – BJT amplifier using BC 547 where β = 300 & $V_{BE}$ = 0.7 V. Calculate the input resistance ($R_i$), output resistance ($R_o$) & small signal voltage gain ($A_v$).<br>  <br>**Fig. 3 for Q.3 (C)** |

# University of Mumbai
## Examination 2020 under Cluster 06
## (Lead College :- Vidyavardhini's College of Engineering & Technology)

**Examinations Commencing from 7th January 2021 to 20th January 2021**

Program: **Electronics Engineering**

Curriculum Scheme: Rev. 2019

Examination: S.E. Semester III

Course Code: ELC302 and Course Name: Electronic Devices & Circuits – I

Time: 2 hour Max. Marks: 80

---

**Q.1**

| Question No. | Correct Option (Enter either 'A' or 'B' or 'C' or 'D') |
|---|---|
| Q.1 | D |
| Q.2 | B |
| Q.3 | A |
| Q.4 | A |
| Q.5 | D |
| Q.6 | A |
| Q.7 | B |
| Q.8 | C |
| Q.9 | B |
| Q.10 | D |
| Q.11 | C |
| Q.12 | D |
| Q.13 | A |
| Q.14 | B |
| Q.15 | C |
| Q.16 | D |
| Q.17 | C |

| | |
|---|---|
| Q.18 | D |
| Q.19 | A |
| Q.20 | A |

**Q.2 (A) - Explain the effects of temperature on the V – I characteristics of PN junction diode with a neat sketch / diagram & appropriate mathematical expressions.**

★ EFFECT OF TEMP. ON DIODE CHARACTERISTICS :-

As we know that the forward current through diode is given by eqn :

$$I_f = I_s \left(e^{V_D/\eta V_T} - 1\right)$$

For the values of $V_D$ $e^{V_D/\eta V_T} >> 1$.

$$\therefore I_f = I_s e^{V_D/\eta V_T}$$

$$\therefore \frac{I_f}{I_s} = e^{V_D/\eta V_T}$$

∴ Taking $\log_e$ on both sides, we get

$$\log_e e^{V_D/\eta V_T} = \log_e \left(\frac{I_f}{I_s}\right)$$

$$\therefore \frac{V_D}{\eta \cdot V_T} \log_e e = \log_e \left(\frac{I_f}{I_s}\right)$$

$$\therefore \frac{V_D}{\eta V_T} = \log_e\left(\frac{I_f}{I_s}\right)$$

$$\therefore V_D = \eta V_T \log_e\left[\frac{I_f}{I_s}\right] \longrightarrow (A)$$

The above Equation indicates that forward voltage drop across diode depends upon the Reverse saturation current Is. The reverse saturation current Is of diode doubles in magnitude for every 10°C increase in temp., it means that increase in temp. increases Is, and hence forward voltage drop $V_D$ across diode decreases. From the equation (A), $V_D$ also depends upon the $V_T$, but change in $V_T$ due to temp. is comparatively less as change in Is. Thus increase in level of Is, will overpower the smaller percentage change in $V_T$.

Thus as the temp. of the diode increases then the forward voltage drop i.e $V_D$ decreases, hence, diode conducts earlier, due to which the forward characteristics of the diode moves to the left with increase in temperature.

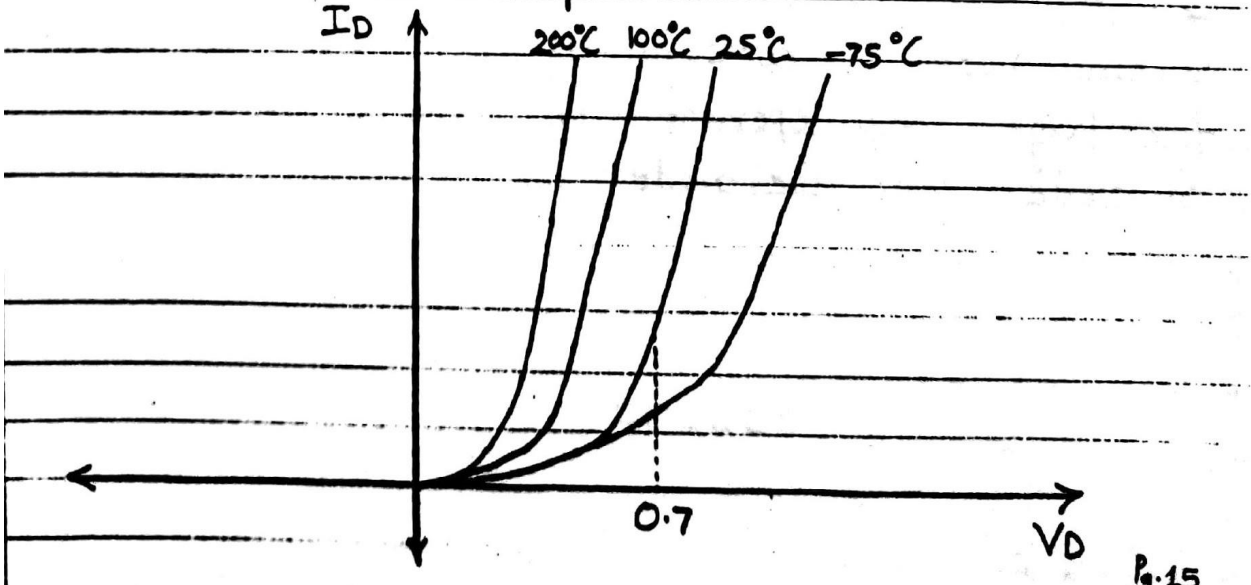



Fig. 15

**Q.3 (A) – For the voltage divider bias circuit shown in Fig. 1 using silicon (Si) BJT with β = 100 calculate the Q – point where Q = [$V_{CE}$, $I_C$].**

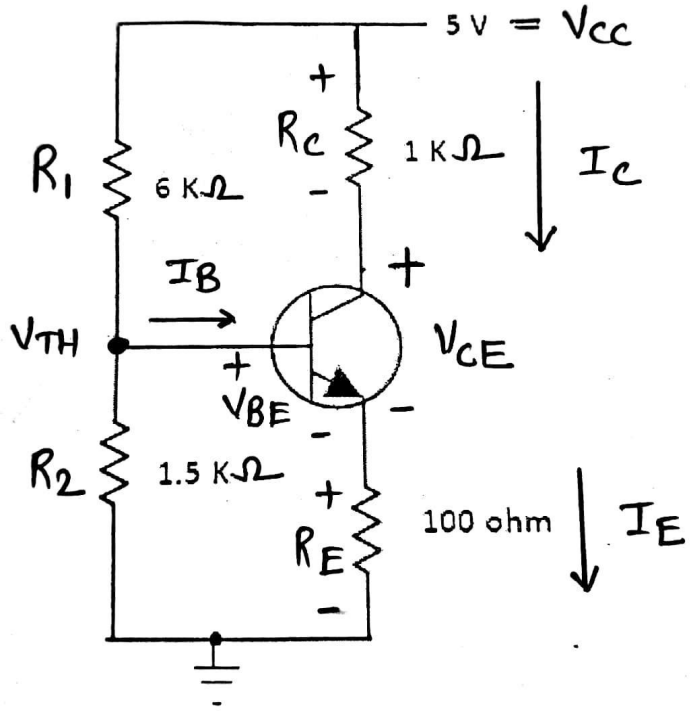



**Fig. 1 for Q.3 (A)**

## (2) BJT Voltage Divider Biasing

Data Given :-

$R_1 = 6K\Omega$ & $R_2 = 1.5K\Omega$

$R_C = 1K\Omega$ & $R_E = 100\Omega$

$\beta = 100$ & $V_{BE} = 0.7V$

$$R_{TH} = R_1 // R_2 = 6K // 1.5K = 1.2K\Omega \longrightarrow (1)$$

$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = \frac{5 \times 1.5K}{6K + 1.5K} = 1V \longrightarrow (2)$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta) R_E} = \frac{1 - 0.7}{1.2K + (101) \times 100} = 26.55\,\mu A \longrightarrow (3)$$

$$I_C = \beta \cdot I_B = 100 \times 26.55 \times 10^{-6} = 2.65mA \longrightarrow (4)$$

$$V_{CE} = V_{CC} - I_C [R_C + R_E] = 5 - 2.65[1 + 0.1] = 2.09V$$

Hence $Q = [V_{CE}, I_C] = [2.09V, 2.65mA]$

**Q.3 (B) – For the voltage divider bias circuit as shown in Fig. 2 using N-channel E-MOSFET calculate the Q – point where Q = [$V_{DS}$, $I_D$].**

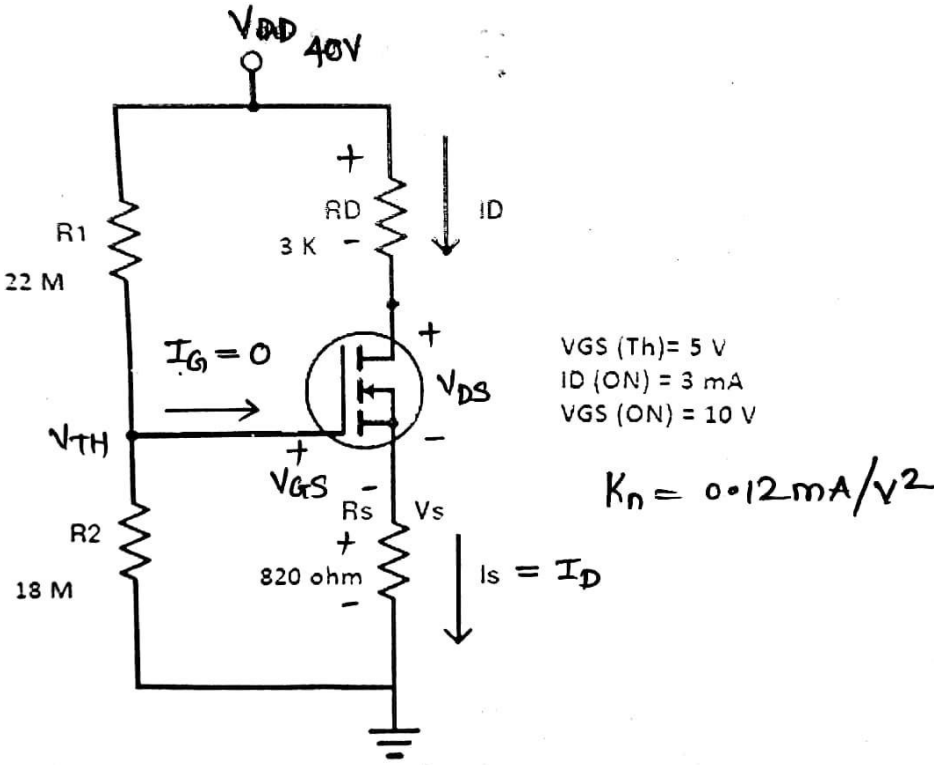



**Fig. 2 for Q.3 (B)**

E-MOSFET voltage Divider Biasing

$$K_n = \frac{I_{D(ON)}}{[V_{GS(ON)} - V_{GS(TH)}]^2} = \frac{3mA}{[10-5]^2} = 0.12\,mA/V^2 \longrightarrow (1)$$

$$V_{GS} = V_{TH} - I_D R_S = 18 - 0.82 I_D \longrightarrow (2)$$

$$I_D = K_n [V_{GS} - V_{GS(TH)}]^2 \longrightarrow (3)$$

$$I_D = 0.12 [18 - 0.82 I_D - 5]^2 \longrightarrow (4)$$

$$\boxed{\text{Hence } I_D = 6.725\,mA} \longrightarrow (5)$$

$$V_{DS} = V_{DD} - I_D [R_D + R_S] = 40 - 6.725 [3 + 0.82] \longrightarrow (6)$$

$$\boxed{\text{Hence } V_{DS} = 14.31\,V}$$

Hence the Q-point is located at $Q = [V_{DS}, I_D]$

$$Q = [14.31V, 6.725mA]$$

**Q.3 (C) - Fig. 3 shows a single stage CE – BJT amplifier using BC 547 where β = 300 & $V_{BE}$ = 0.7 V. Calculate the input resistance ($R_i$), output resistance ($R_o$) & small signal voltage gain ($A_v$).**

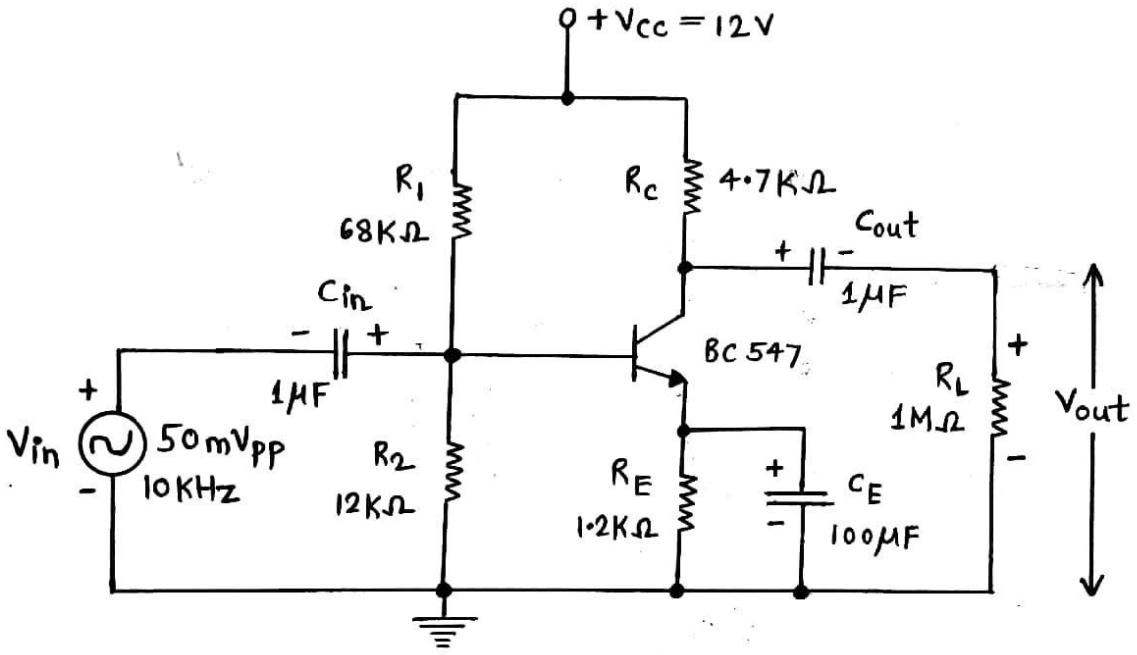



**Fig. 3 for Q.3 (C)**

Q.2(a) DC operating conditions :-

$$V_{TH} = \frac{V_{CC} \cdot R_2}{R_1 + R_2} = \frac{12 \times 12K}{12K + 68K} = 1.8\,V \longrightarrow (1)$$

$$R_{TH} = R_1 /\!/ R_2 = 68K /\!/ 12K = 10.2\,K\Omega \longrightarrow (2)$$

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta)R_E} = \frac{1.8 - 0.7}{10.2K + (1+300) \times 1.2K} = 2.96\,\mu A \longrightarrow (3)$$

$$r_\pi = \frac{26\,mV}{I_B} = \frac{26 \times 10^{-3}}{2.96 \times 10^{-6}} = 8.783\,K\Omega \longrightarrow (4)$$

AC operating conditions :-

$$R_i = R_1 /\!/ R_2 /\!/ r_\pi = 68K /\!/ 12K /\!/ 8.78K = 4.72\,K\Omega \longrightarrow (5)$$

$$R_o = R_c = 4.7\,K\Omega \longrightarrow (6)$$

$$R_{eq} = R_E /\!/ \left[\frac{r_\pi}{1+\beta}\right] = 1.2K /\!/ 29.28 = 28.58\,\Omega \longrightarrow (7)$$

$$|A_v| = \left[R_c /\!/ R_L\right]\left[\frac{1+\beta}{r_\pi}\right] = 160.32 \longrightarrow (8)$$