University of Mumbai
Examination 2021 under Cluster 06
(Lead College: Vidyavardhini's College of Engg Tech)

Examinations Commencing from 15th June 2021

Program: **Electronics Engineering**

Curriculum Scheme: Rev 2019

Examination: SE Semester III

Course Code: ELC303 and Course Name: Digital Logic Circuits

Time: 2 hours Max. Marks: 80

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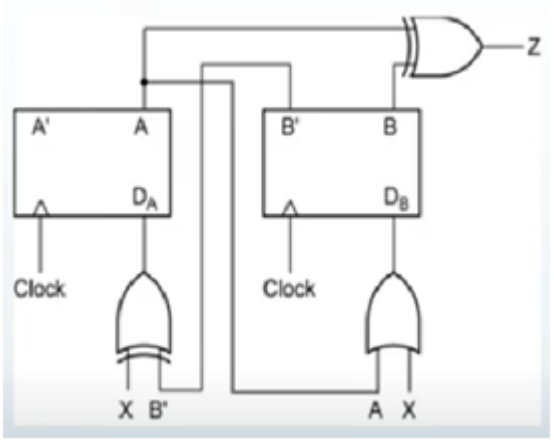
Q1.	**Choose the correct option for following questions. All the Questions are compulsory and carry equal marks**
1.	Convert $(11011.101)_2$ binary to decimal.
Option A:	$(26.625)_{10}$
Option B:	$(27.125)_{10}$
Option C:	$(27.625)_{10}$
Option D:	$(26.125)_{10}$
2.	Convert Gray code (10110010) to Binary code
Option A:	$(11101011)_2$
Option B:	$(11011100)_2$
Option C:	$(11011101)_2$
Option D:	$(11101001)_2$
3.	Simplified form of the Boolean expression $X(YZ + \overline{Y}Z)$
Option A:	XYZ
Option B:	XY
Option C:	XZ
Option D:	YZ
4.	The logic expression f = ABC+ ĀBC+ ĀBC is in
Option A:	SOP form
Option B:	POS form
Option C:	Standard SOP form
Option D:	Standard POS form
5.	The logic gate used in parity checker is a
Option A:	NAND Gate
Option B:	NOR Gate
Option C:	Ex-OR Gate
Option D:	AND Gate
6.	IC 74151 is a
Option A:	4:1 multiplexer
Option B:	8:1 multiplexer
Option C:	16:1 multiplexer

Option D:	32:1 multiplexer
7.	Which logic gate is a basic comparator
Option A:	NOR Gate
Option B:	NAND gate
Option C:	X-OR Gate
Option D:	X-NOR Gate
8.	Convert JK flip-flop to D flip-flop
Option A:	J=D, K=0
Option B:	J=1, K=D
Option C:	J=D, $K = \overline{D}$
Option D:	J=0, $K = \overline{D}$
9.	An ‘n’ Flip-Flop Ring counter can have
Option A:	n states
Option B:	2n states
Option C:	(n-1) states
Option D:	(n+1)states
10.	When the JK flip-flop is set , it’s inputs will be
Option A:	J=0, K=0
Option B:	J=0, K=1
Option C:	J=1, K=0
Option D:	J=1, K=1
11.	IC 7490 consist of
Option A:	MOD 6 and MOD 2 counter
Option B:	MOD 5 and MOD 2 counter
Option C:	MOD 8 and MOD 2 counter
Option D:	MOD 5 and MOD 3 counter
12.	In IC74163, if CLR=ENP=ENT=1 , LD=0, ABCD=0011, What is Output at pin QD, QC,QB,QA
Option A:	1100
Option B:	0011
Option C:	0101
Option D:	0010
13.	In machine the output depends on Present state and external input.
Option A:	Mealy
Option B:	Sequential asynchronous
Option C:	Asynchronous
Option D:	Moore
14.	Which of the Logic family dissipate minimum power
Option A:	TTL
Option B:	CMOS
Option C:	DTL
Option D:	ECL

15.	Recommended fan out for TTL is
Option A:	10
Option B:	4
Option C:	20
Option D:	30
16.	FPGA stands for
Option A:	Field Programmable Gate Application
Option B:	Field Programmable Gate Array
Option C:	Field Programmable Gala Array
Option D:	FET Programmable Gate Array
17.	Figure of merit of IC family is
Option A:	Gate propagation delay
Option B:	Gate power Dissipation
Option C:	Speed power product
Option D:	Fan out
18.	In Verilog, function always execute
Option A:	Zero Time
Option B:	Non-Zero Time
Option C:	One millisecond
Option D:	One microsecond
19.	Operator symbol <<< is a
Option A:	Arithmetic shift left
Option B:	Arithmetic shift right
Option C:	Logical shift left
Option D:	Logical shift right
20.	Operator <= is used for
Option A:	Blocking assignment
Option B:	Non-Blocking assignment
Option C:	Single line comment
Option D:	Multiple line comments

Q.2 (20 Marks)	
Q2.A	**Solve any Two 5 marks each**
i.	Minimize the following expression using k-map and implement using basic gates. $F(A,B,C,D)=\sum m(1,7,9,10,11,15)+ d(2,3,5)$
ii.	Write short note on CPLD Architecture.
iii.	Write Verilog code for 4:1multiplexer in Data Flow modeling.

Q2.B	**Solve any One 10 marks each**
i.	Design and implement MOD 6 Asynchronous counter using T flip-flops.
ii.	Analyze the given state machine and draw the state diagram. 
Q.3 (20 Marks)	
Q3.A	**Solve any Two 5 marks each**
i.	Write short note on Hamming code.
ii.	Implement following function using PLA. F1=∑m (0,3,4,7) F2=∑m (1,2,5,7)
iii.	Write Verilog code for D flip-flop in behavioral modeling with asynchronous reset.
Q3.B	**Solve any One 10 marks each**
i.	Design and Implement Full adder circuit using a 3:8 decoder IC 74138.
ii.	Explain universal shift register. Design and implement Twisted ring counter using IC 74194.

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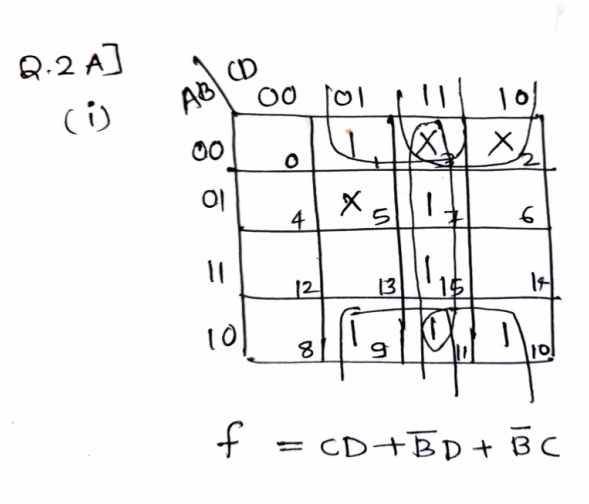
Q1:

Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	C
Q2.	B
Q3.	C
Q4	C
Q5	C
Q6	B
Q7	D
Q8.	C
Q9.	A
Q10.	C
Q11.	B
Q12.	A
Q13.	A
Q14.	B
Q15.	A
Q16.	B
Q17.	C
Q18.	A
Q19.	A
Q20.	B

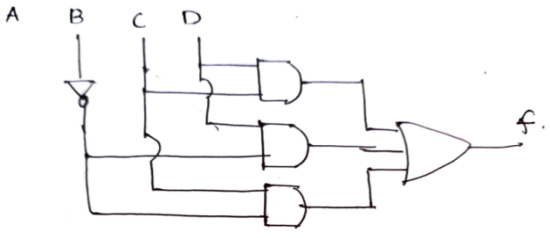
Important steps and final answer for the questions involving numerical example

Q2(A): (i)

Step 1 Enter minterms in k map and minimize expression



Step2 Implement using basic gates



Q.2A(iii)

```
module m41 ( input a,
input b,
input c,
input d,
input s0, s1,
output out);
 assign out = s1 ? (s0 ? d
: c) : (s0 ? b : a);


endmodule
```

Q.2B(i)Step1: T MOD 6 synchronous counter will require 3 flip flops and will count from 000 to 101. Rest of the states are invalid. To design the combinational circuit of valid states, following truth table and K-map is drawn:

Q_C	Q_B	Q_A	Reset logic
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

Fig1. Truth table of MOD 6 asynchronous counter

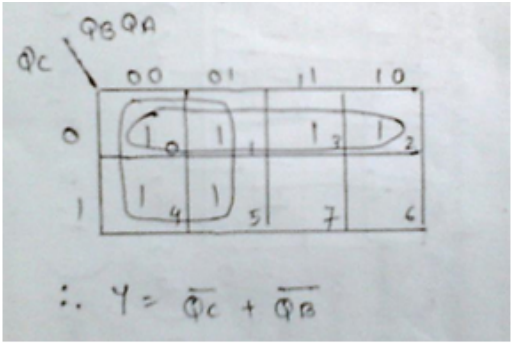


Fig2. K-map for above truth table

Thus reset logic is OR of complemented forms of QC and QB. This will be given to the reset inputs of the counter so that as soon as count 110 reaches, the counter will reset. Thus the counter will count from 000 to 101. The implementation of the designed MOD 6 asynchronous counter is shown below

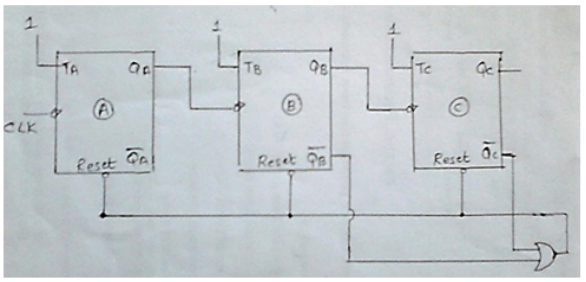


Fig3. Circuit diagram of MOD 6 asynchronous counter

Q.2B(ii)

Step1:Moore machine

Step2 :Equations

$$A^+ = D_A = X \oplus B'$$
$$B^+ = D_B = A+X$$

Z=A XOR B

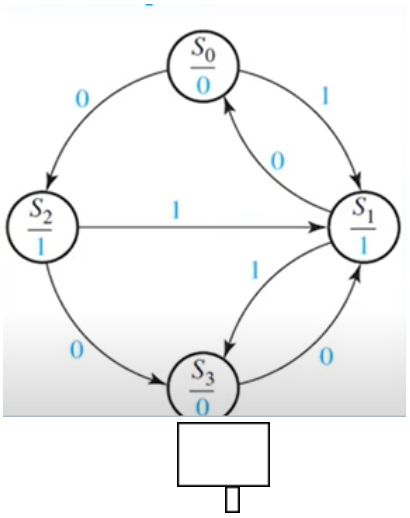
Step3:State transition table

Present State AB	Input X	Next State A^+B^+	Current Output Z
00	0	10	0
	1	01	
01	0	00	1
	1	11	
10	0	11	1
	1	01	
11	0	01	0
	1	11	

Step 4: State assignment

S_0=00, S_1=01,S_2=10,S_3=11

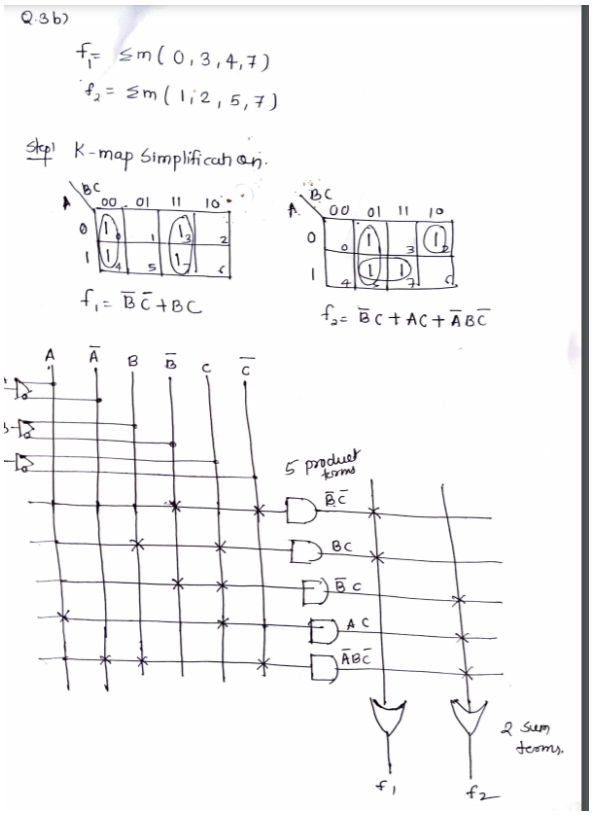
Step 5: State Diagram

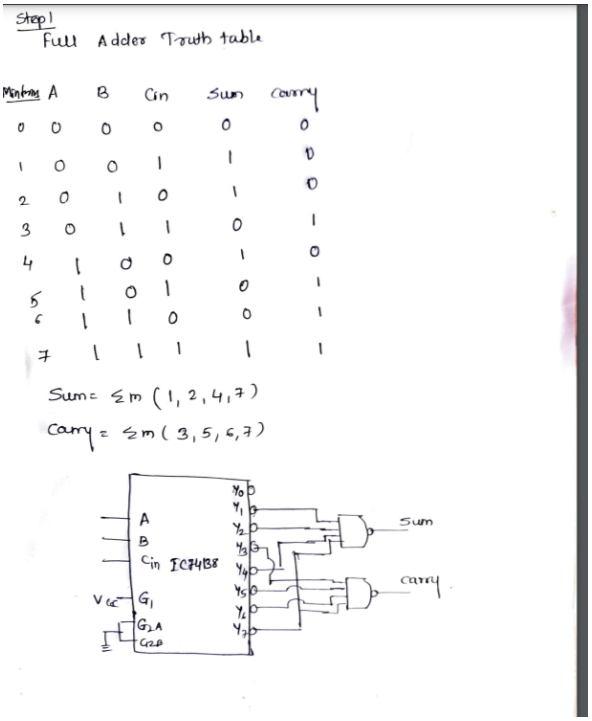



```
always@(posedge clk or
posedge clear)
begin
if(clear== 1)
q <= 0;
qbar <= 1;
else
q <= d;
qbar = !d;
end
endmodule
```

Q.3B(I)

Q.3A(ii)





Q.3 B(ii)

Q.3a(iii)

```
module
dff_behavioral(d,clk,clear,
q,qbar);
input d, clk, clear;
output reg q, qbar;
```

Function	Inputs S1	Inputs S0	Next state QA^n	Next state QB^n	Next state QC^n	Next state QD^n
Hold	0	0	QA	QB	QC	QD
Shift right	0	1	RIN	QA	QB	QC
Shift left	1	0	QB	QC	QD	LIN
Load	1	1	A	B	C	D

Johnson Counter ("Twisted ring" counter)