University of Mumbai
Examination June 2021
Examinations Commencing from 1st June 2021
Program: **Computer Engineering**
Curriculum Scheme: Rev2019
Examination: SE Semester IV
Course Code: CSC405 and Course Name: Microprocessor

Time: 2 hour   Max. Marks: 80

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Q1.	Choose the correct option for following questions. All the Questions are compulsory and carry equal marks
1.	In protected mode of 80386, the VM flag is set by using
Option A:	IRET instruction or task switch operation
Option B:	IRET instruction
Option C:	Task switch operation
Option D:	NOP
2.	The instructions that are used for reading an input port and writing an output port respectively are
Option A:	MOV, XCHG
Option B:	MOV, IN
Option C:	IN, MOV
Option D:	IN, OUT
3.	While CPU is executing a program, an interrupt exists then it
Option A:	follows the next instruction in the program
Option B:	jumps to instruction in other registers
Option C:	breaks the normal sequence of execution of instructions
Option D:	stops executing the program
4.	8086 can access up to?
Option A:	512KB

Option B:	1MB
Option C:	2MB
Option D:	256KB
5.	Because of Pentium's superscalar architecture, the number of instructions that are executed per clock cycle is
Option A:	1
Option B:	2
Option C:	3
Option D:	4
6.	The paging unit is enabled only in
Option A:	virtual mode
Option B:	addressing mode
Option C:	protected mode
Option D:	Real Mode
7.	In 8257 register format, the selected channel is disabled after the terminal count condition is reached when
Option A:	Auto load is set
Option B:	Auto load is reset
Option C:	TC STOP bit is reset
Option D:	TC STOP bit is set
8.	All the functions of the ports of 8255 are achieved by programming the bits of an internal register called
Option A:	data bus control
Option B:	read logic control
Option C:	control word register
Option D:	Status Register
9.	When non-specific EOI command is issued to 8259A it will automatically

Option A:	set the ISR
Option B:	reset the ISR
Option C:	set the INTR
Option D:	reset the INTR
10.	For a single task in protected mode, the 80386 can address the virtual memory of
Option A:	32 GB
Option B:	64 MB
Option C:	32 TB
Option D:	64 TB
11.	The recurrence of the numerical values or constants in a program code is reduced by
Option A:	EQU
Option B:	ASSUME
Option C:	LOCAL
Option D:	LABEL
12.	The hyperthreading technology automatically involves the
Option A:	decrease of die area
Option B:	increase of die area
Option C:	decrease of die area to half
Option D:	increase of die area to half
13.	The 80386 enables itself to organize the available physical memory into pages, which is known as
Option A:	segmentation
Option B:	Paging
Option C:	memory division
Option D:	Virtual memory

14.	The number of debug registers that are available in 80386, for hardware debugging and control is
Option A:	2
Option B:	4
Option C:	8
Option D:	16
15.	The instruction, JMP 5000H:2000H; is an example of
Option A:	intrasegment direct mode
Option B:	intrasegment indirect mode
Option C:	intersegment direct mode
Option D:	intersegment indirect mode
16.	The salient feature of Pentium is
Option A:	superscalar architecture
Option B:	superpipelined architecture
Option C:	superscalar and superpipelined architecture
Option D:	multiple instruction issue
17.	The speed of integer arithmetic of Pentium is increased to a large extent by
Option A:	on-chip floating point unit
Option B:	superscalar architecture
Option C:	4-stage pipelines
Option D:	instruction cache
18.	For 8086 microprocessor, the stack segment may have a memory block of a maximum of
Option A:	32K bytes
Option B:	64K bytes
Option C:	16K bytes

Option D:	128K bytes
19.	Which of the following is not a module of Pentium 4 architecture?
Option A:	front end module
Option B:	execution module
Option C:	control module
Option D:	Memory subsystem module
20.	The type of the interrupt may be passed to the interrupt structure of CPU from
Option A:	interrupt service routine
Option B:	Stack
Option C:	interrupt controller
Option D:	Segments

Q2	Solve any Four out of Six 5 marks each
A	Explain different types of Interrupts? Explain Interrupt Vector table for 8086
B	Draw and explain the internal block diagram of 8257? How DMA operations are performed?
C	Explain what is Branch Prediction Logic in Pentium? Explain working of Branch Prediction with suitable diagram?
D	Compare the 8086, 80386, Pentium Processor.
E	Draw and explain the internal architecture of 80386 microprocessor?
F	Explain the operating modes of 80386?

Q3.	Solve any Two Questions out of Three 10 marks each
A	Explain the internal architecture of 8086 microprocessor? Differentiate the functioning of Minimum mode and Maximum mode?
B	Write an assembly language program to find the largest number from an

	unordered array of 8-bit numbers?
C	Interface 32K word of memory to 8086 microprocessor system. Available memory chips are 16K*8 RAM. Use suitable decoder for generating chip logic.

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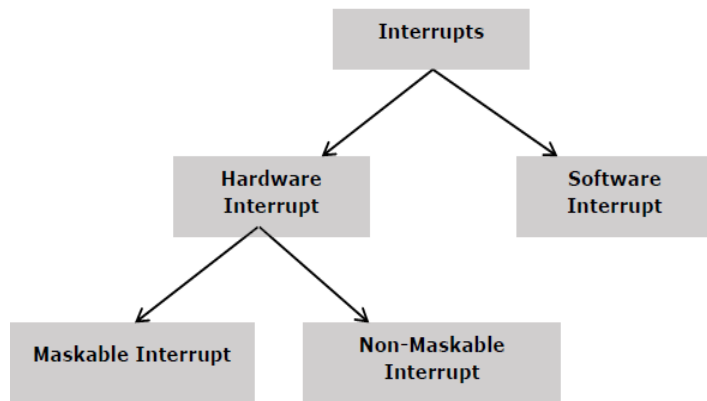Course Code: CSC405 and Course Name: Microprocessor

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Question Number	Correct Option (Enter either 'A' or 'B' or 'C' or 'D')
Q1.	A
Q2.	D
Q3.	C
Q4	B
Q5	B
Q6	C
Q7	D
Q8.	C
Q9.	B
Q10.	D
Q11.	A
Q12.	B
Q13.	B
Q14.	C
Q15.	C
Q16.	C
Q17.	C
Q18.	B
Q19.	C
Q20.	C

Q2

Answer A

Different types of interrupt in 8086:*(2 Marks)*

Interrupt Vector Table to be explained *(3 Marks)*

Answer B

8257 Architecture*(3 Marks)*
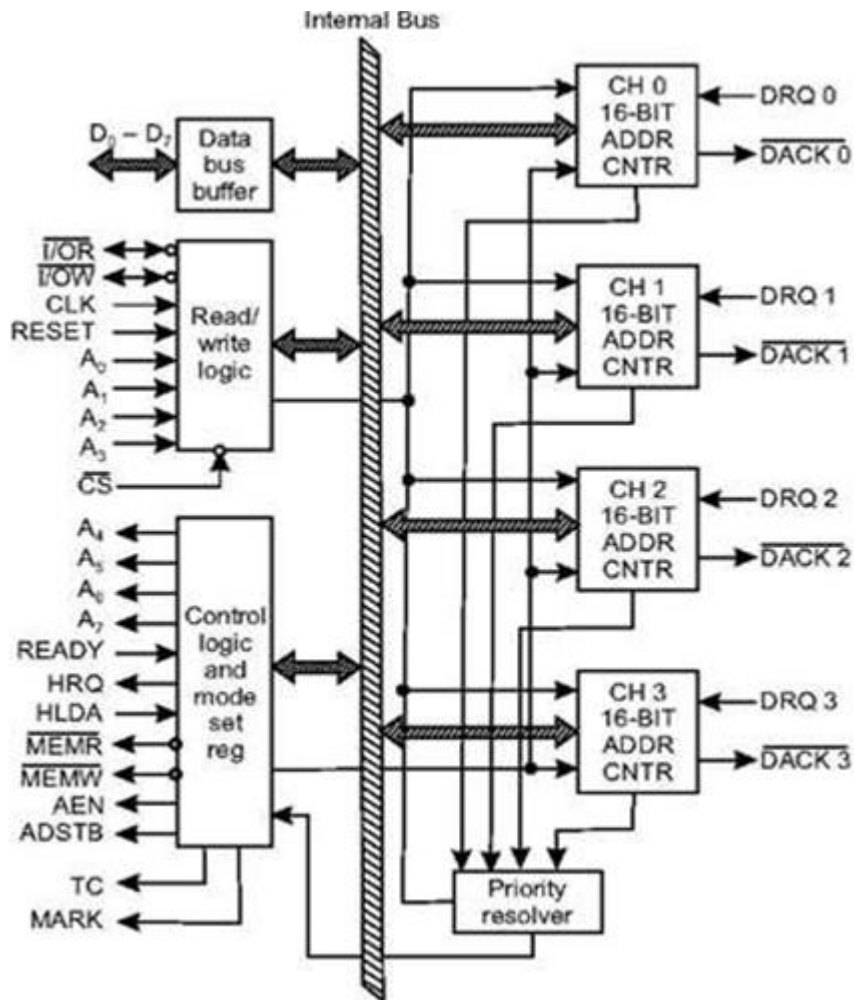
Following are the operations performed by a DMA:*(2 Marks)*

- Initially, the device has to send DMA request (DRQ) to DMA controller for sending the data between the device and the memory.

- The DMA controller sends Hold request (HRQ) to the CPU and waits for the CPU for the HLDA.

- When CPU gets the HLDA signal then, it leaves the control over the bus and acknowledges the HOLD request through HLDA signal.

- Now the CPU is in the HOLD state and the DMA controller has to manage the operations over the buses between the CPU, memory and I/O devices.

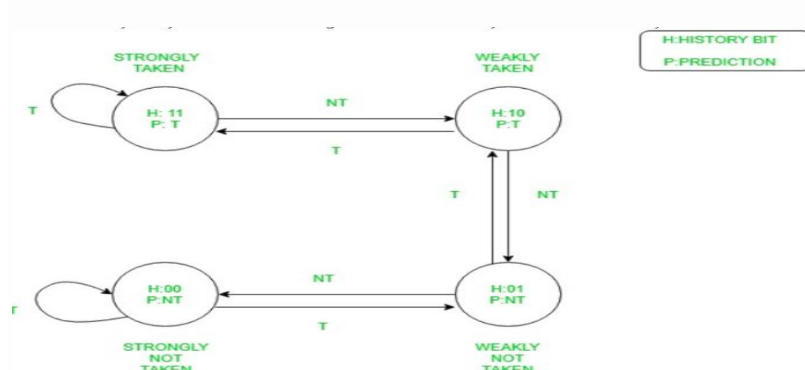**Answer C**

Branch prediction logic: (*2 Marks*)

To avoid this problem, Pentium uses a scheme called Dynamic Branch Prediction. In this scheme, a prediction is made for the branch instruction currently in the pipeline. The prediction will either be taken or not taken. If the prediction is true then the pipeline will not be flushed and no clock cycles will be lost. If the prediction is false then the pipeline is flushed and starts over with the current instruction.

It is implemented using 4 way set associated cache with 256 entries. This is called Branch Target Buffer (BTB). The directory entry for each line consists of:

- Valid bit: Indicates whether the entry is valid or not.

- History bit: Track how often bit has been taken.

Source memory address is from where the branch instruction was fetched. If the directory entry is valid then the target address of the branch is stored in corresponding data entry in BTB.

Working of Branch Prediction:(*3 Marks*) *{Explanation with diagram}*

Answer D *(Any 5-6 points can be included)*

| Product	8086	80386	Pentium
Year introduced	1978	1985	1992
Technology	NMOS	CMOS	BICMOS
Clock rate (MHz)	3 - 10	16 - 33	60, 66
Number of pins	40	132	273
Number of transistors	29,000	275,000	3.1 million
Physical memory	1M	4G	4G
Virtual memory	None	64T	64T
Internal data bus	16	32	32
External data bus	16	32	64
Address bus	20	32	32
Data type (bits)	8, 16	8, 16, 32	8, 16, 32

Answer E

Explanation:(*2 Marks)*

The six functional units of the 80386 Architecture are

- Bus Interface Unit
- Code Pre-fetch Unit
- Instruction Decoder Unit
- Execution Unit
- Segmentation Unit
- Paging Unit

Diagram:(*3 Marks)*
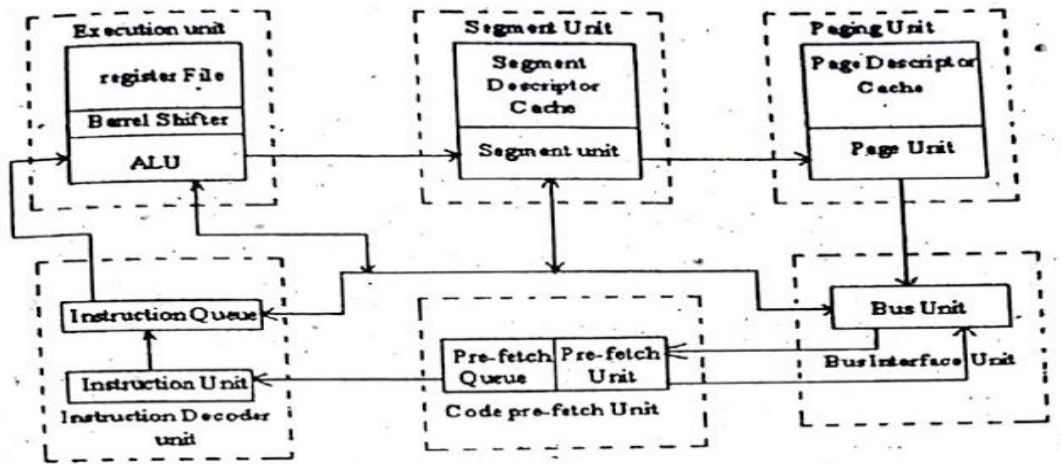
Answer F

1. Real Mode

2. Protected Mode

3. Virtual Mode

Modes to be described in brief.

Q3

Answer A

Architechture(*5 Marks***) :-***Block Diagram(3 Marks) Explanation (2 Marks)*

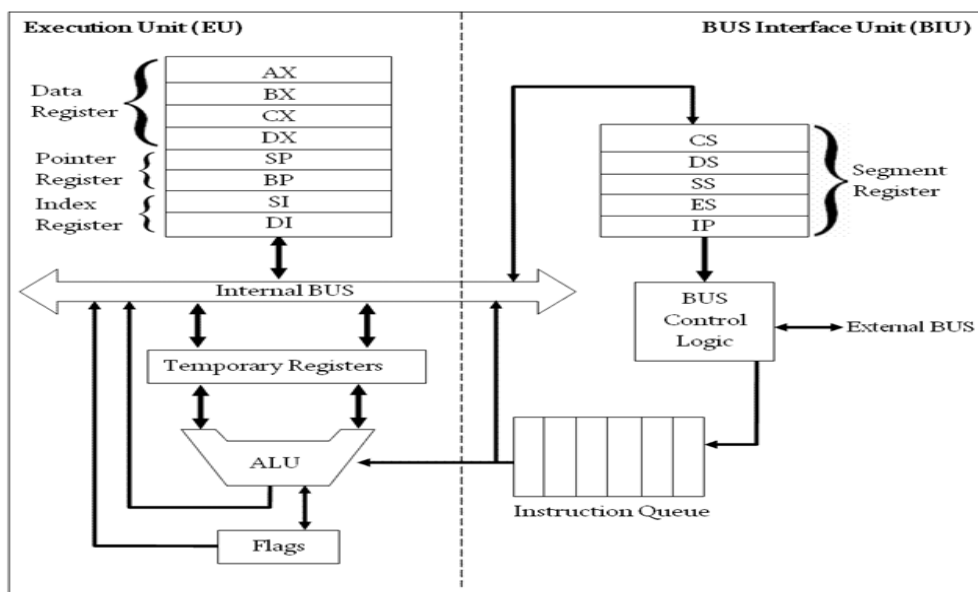8086 contains two independent functional units: a Bus Interface Unit (BIU) and an Execution Unit (EU).

Fig: Block Diagram of Intel 8086 Microprocessor (8086 Architecture)

Distinguish(*5 Marks)(Any 5-6 points can be included)*

Minimum mode	Maximum mode
In minimum mode there can be only one processor i.e. 8086.	In maximum mode there can be multiple processors with 8086, like 8087 and 8089.
$\overline{MN/MX}$ is 1 to indicate minimum mode.	$\overline{MN/MX}$ is 0 to indicate maximum mode.
ALE for the latch is given by 8086 as it is the only processor in the circuit.	ALE for the latch is given by 8288 bus controller as there can be multiple processors in the circuit.
$\overline{DEN}$ and $\overline{DT/R}$ for the trans-receivers are given by 8086 itself.	and $\overline{DT/R}$ for the trans-receivers are given by 8288 bus controller.
Direct control signals $\overline{M/IO}$, $\overline{RD}$ and $\overline{WR}$ are given by 8086.	Instead of control signals, each processor generates status signals called $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$.
Control signals $\overline{M/IO}$, $\overline{RD}$ and $\overline{WR}$ are decoded by a 3:8 decoder like 74138.	Status signals $\overline{S2}$, $\overline{S1}$ and $\overline{S0}$ are decoded by a bus controller like 8288 to produce control signals.
$\overline{INTA}$ is given by 8086 in response to an interrupt on INTR line.	$\overline{INTA}$ is given by 8288 bus controller in response to an interrupt on INTR line.
HOLD and HLDA signals are used for bus request with a DMA controller like 8237.	$\overline{RQ}/\overline{GT}$,lines are used for bus requests by other processors like 8087 or 8089.
The circuit is simpler.	The circuit is more complex.

Multiprocessing cannot be performed hence performance is lower.	As multiprocessing can be performed, it can give very high performance.

Answer B

Assembly language program to find the largest number*(6Marks)*
Output *(2 Marks)*
Algorithm / Flowchart*(2 Marks)*

Answer C

Step 1*(2Marks)*

Step 2*(1Marks)*

Step 3*(3Marks)*

Step 4*(4Marks)*

Step_1: Total memory = 32 K word = 32*2 K = 64 K
        IC available = 16 K
        hence,
        number of RAM IC required = 64 K x 8/ 16 Kx8 = 4 ICs
        so,
            EVEV Bank = 2 ICs of 16 Kx8 RAM
            ODD Bank = 2 ICs of 16 Kx8 RAM

Even bank	Odd bank
RAM _1 (16K)	RAM _2 (16K)
RAM_ 3 (16K)	RAM _4 (16K)

Step_2: Number of address lines required = 15 address lines

Step_3: Address decoding table

MEMORY IC	HEX ADDRESS	BINARY ADDRESS																			
		A_{19}	A_{18}	A_{17}	A_{16}	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
16 K x 8 RAM-(1)	00000	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	07FFE	O	O	O	O	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	O
16 K x 8 RAM-(3)	8000	O	O	O	O	1	O	O	O	O	O	O	O	O	O	O	O	O	O	O	O
	0FFFE	O	O	O	O	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	O

To decoder   To 16 K IC

Step_3: Generation of chip select logic

A_{18} A_{19} M / $\overline{IO}$
  0   0   1
E_1 $\overline{E_2}$ E_3

A_{17} → A
A_{16} → B   3:8
A_{15} → C   Decoder
                 74LS373

Y_0 → To $\overline{CS_0}$
Y_1 → To $\overline{CS_1}$
Y_2
Y_3
Y_4
Y_5
Y_6
Y_7