## University of Mumbai

## Examination June 2021

Examinations Commencing from 1 ${ }^{\text {st }}$ June 2021
Program: BE Electronics and Telecommunication
Curriculum Scheme: Rev2019 C-Scheme
Examination: SE Semester IV
Course Code: ECC402 and Course Name: Microcontrollers
Time: 2 hour
Max. Marks: 80

| Q1. | Choose the correct option for following questions. All the Questions are compulsory and carry equal marks |
| :---: | :---: |
| 1. | Which of the following parts of the microprocessor is closely related to register? |
| Option A: | Processor |
| Option B: | ALU |
| Option C: | CPU |
| Option D: | Memory |
| 2. | During the execution of a program, which register is initialized first? |
| Option A: | Instruction registers |
| Option B: | Program Counter |
| Option C: | Stack pointer |
| Option D: | Program status word |
| 3. | A microprocessor is clocked at a rate of 3 GHz . How long is a clock cycle? |
| Option A: | 0.2 ns |
| Option B: | 0.3n |
| Option C: | 1.5 ns |
| Option D: | 1 ns |
| 4. | How can we change the speed of a DC motor using PWM in PIC 16 F 886 microcontroller? |
| Option A: | By changing amplitude of Pulse |
| Option B: | By keeping fixed duty cycle |
| Option C: | By changing duty cycle |
| Option D: | By increasing power of Pulse |
| 5. | A CPU generates 32 -bit virtual addresses. The page size is 4 KB . The processor has a translation look-aside buffer (TLB), which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is: |
| Option A: | 11 bits |
| Option B: | 13 bits |
| Option C: | 15 bits |
| Option D: | 20 bits |
| 6. | The high speed memory between the CPU and main memory is called as------- |
| Option A: | Cache Memory |
| Option B: | Virtual memory |
| Option C: | Secondary memory |
| Option D: | Storage memory |


| 7. | The register that can be used as a scratch pad in 8051 is |
| :---: | :---: |
| Option A: | Accumulator |
| Option B: | Stack Pointer |
| Option C: | Program Counter |
| Option D: | B register |
| 8. | The registers that provide control and status information about Timer/Counters in 8051 is |
| Option A: | IP, IE |
| Option B: | TMOD, TCON |
| Option C: | SCON,SBUF |
| Option D: | Flag register, Accumulator |
| 9. | The higher and lower bytes of a 16-bit register DPTR in 8051 are represented respectively as |
| Option A: | LDPTR and HDPTR |
| Option B: | DPTRL and DPTRH |
| Option C: | DPH and DPL |
| Option D: | HDP and LDP |
| 10. | The pin that is grounded for interfacing external program memory in 8051 is |
| Option A: | EA(active low) |
| Option B: | PSEN(active low) |
| Option C: | OE(active low) |
| Option D: | ALE |
| 11. | The 8051 instruction that is used to complement or invert the bit of a bit addressable SFR is |
| Option A: | CLR C |
| Option B: | CPL C |
| Option C: | CPL Bit |
| Option D: | ANL Bit |
| 12. | The first byte of an absolute jump instruction in 8051 consists of |
| Option A: | 3 LSBs of opcode and 5 MSBs of 11-bit address |
| Option B: | 5 LSBs of opcode and 3 MSBs of 11-bit address |
| Option C: | 5 MSBs of opcode and 3 LSBs of 11-bit address |
| Option D: | 6 MSBs of opcode and 1 LSB of 11-bit address |
| 13. | What is the function of a watchdog timer (WDT)? |
| Option A: | It resets the system if applied voltage increased above threshold value |
| Option B: | It resets the system if applied voltage decreases below threshold value |
| Option C: | It resets the system if the software fails to operate properly. |
| Option D: | It resets the system if Power failure is detected. |
| 14. | The instructions that change the sequence of execution are |
| Option A: | conditional instructions |
| Option B: | logical instructions |
| Option C: | control transfer instructions |


| Option D: | data transfer instructions |
| :---: | :--- |
|  |  |
| 15. | In the instruction "MOV TH1, \#-3", what is the value that is being loaded in the <br> TH1 register? |
| Option A: | 0xFCH |
| Option B: | 0xFBH |
| Option C: | 0xFDH |
| Option D: | 0xFEH |
|  |  |
| 16. | How many registers are there in ARM7? |
| Option A: | 35 register( 28 GPR and 7 SPR) |
| Option B: | 37 registers(28 GPR and 9 SPR) |
| Option C: | 37 registers(31 GPR and 6 SPR) |
| Option D: | 35 register(30 GPR and 5 SPR) |
|  |  |
| 17. | How much flash memory does the Atmega328 have? |
| Option A: | 13 K bytes |
| Option B: | 32 K bytes |
| Option C: | 256 K bytes |
| Option D: | 16 K bytes |
|  |  |
| 18. | What is the capability of ARM7 instruction for a second? |
| Option A: | 110 MIPS |
| Option B: | 130 MIPS |
| Option C: | 150 MIPS |
| Option D: | 125 MIPS |
|  |  |
| 19. | Which of the following are pipelining stages of ARM7? |
| Option A: | Fetch, Decode, Write |
| Option B: | Fetch, Decode, Execute, Write |
| Option C: | Fetch, Execute, Write |
| Option D: | Fetch, Decode, Execute |
|  |  |
| 20. | In ARM 7, program counter is implemented using |
| Option A: | Caches |
| Option B: | Heaps |
| Option C: | General purpose register |
| Option D: | Stack |


| Q2 <br> (20 Marks ) | Solve any Four out of Six |
| :---: | :--- |
| A | Compare RISC and CISC architecture. |
| B marks each |  |
| C | Compare microprocessor and microcontroller. |
| D | Explain the concept of cache memory with a diagram. |
| E | Explain the concept of assembler directives in 8051. |
| F | Explain the concept of architectural inheritance in ARM 7. |


| Q3. <br> (20 Marks) | Solve any Two Questions out of Three 10 marks each |
| :---: | :--- |
| A | Write an assembly level language program using 8051 to produce a delay time <br> of 15 seconds if crystal frequency is 11.0592MHz. Use Timer 0 in mode 1. |
| B | Explain in detail the various steps involved in selecting a microcontroller for <br> a given application. |
| C | Explain in detail with diagrams Ports Pin Structure of 8051 microcontroller. |

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| Question <br> Number | Correct Option <br> (Enter either ' $\mathbf{A}^{\prime}$ or ' $\mathbf{B}$ <br> or ' $\mathbf{C}^{\prime}$ or ${ }^{\prime} \mathbf{D}$ ') |
| :---: | :---: |
| Q1. | D |
| Q2. | B |
| Q3. | B |
| Q4 | C |
| Q5 | C |
| Q6 | A |
| Q7 | D |
| Q8. | B |
| Q9. | C |
| Q10. | A |
| Q11. | C |
| Q12. | B |
| Q13. | C |
| Q14. | C |
| Q15. | C |
| Q16. | C |
| Q17. | B |
| Q18. | B |
| Q19. | D |
| Q20. | C |

