K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22

(Autonomous College Affiliated to University of Mumbai)

End Semester Exam

Nov - Dec 2021

Program: (B. Tech) Artificial Intelligence and Data Science

Examination: SY Semester: III

Course Code: 1UAIC304 and Course Name: Digital Logic and Computer Architecture

Duration: 03 Hours Max. Marks: 60

Instructions:

- (1)All questions are compulsory.
- (2)Draw neat diagrams wherever applicable.
- (3)Assume suitable data, if necessary.

| | | Max. Marks | СО | BT level |
|------|--|---------------|-----|----------|
| Q 1 | Solve any six questions out of eight: | 12 | | |
| i) | What is Binary equivalent of given decimal number (56.125) ₁₀ | 02 | CO1 | U |
| ii) | Perform BCD subtraction of given number using 2's complement method. $(83)_{10} - (21)_{10}$ | 02 | CO2 | Ap |
| iii) | Write D flip-flop truth table and its characteristics equation. | 02 | CO3 | U |
| iv) | What is CISC. | 02 | CO4 | R |
| v) | Define Locality of reference | 02 | CO5 | R |

| vi) | Define Data hazards and list it's types? | 02 | CO6 | R |
|-------|---|----|-----|----|
| vii) | Draw 4:1 Multiplexer gate level diagram. | 02 | CO3 | U |
| viii) | Write Double precision floating point number format. | 02 | CO2 | R |
| Q.2 | Solve any four questions out of six. | 16 | | |
| i) | Implement AND gate using NOR gates only. | 04 | CO1 | Ap |
| ii) | Convert (2A3B) _H in IEEE 754 single precision floating point representation. | 04 | CO2 | Ap |
| iii) | Implement Full adder using Half adder circuit. | 04 | CO3 | Ap |
| iv) | Write micro-operation for instruction MOV R2, [4000H]. | 04 | CO4 | U |
| v) | A block set associative cache consists of 64 blocks divided in 4 block set. The main memory contains 4096 blocks, each 128 words of 16-bit length. What is size of main memory and number of address lines. | 04 | CO5 | Ap |
| vi) | If a processor executes 100 instructions in a pipelined (5 stage) processor and unpipelined processor. What is the speedup achieved by pipelining technique if the time taken for each stage is 20ns? | 04 | CO6 | Ap |
| Q.3 | Solve any two questions out of three. | 16 | | |
| i) | State type codes and show with examples steps to convert Binary to Gray and Gray to Binary. | 08 | CO1 | U |
| ii) | Explain hardwired control units and its types. | 08 | CO4 | U |
| iii) | State Cache Mapping Techniques and explain one technique in detail. | 08 | CO5 | U |
| Q.4 | Solve any two questions out of three. | 16 | | |

| i) | Perform (-11X13) ₁₀ using Booth's Multiplication Algorithm. | 08 | CO2 | Ap |
|------|--|----|-----|----|
| ii) | Explain Addressing modes with examples | 08 | CO3 | U |
| iii) | Explain Flynn's Classification | 08 | CO6 | U |