DECEMBER-2019

EXAMINATION TIMETABLE

T.E.(ELECTRONICS)(Sem VI)(Choice Based)

| Days and Dates | Time | Paper Code | Paper |
|---|---|---|---|
| | | | |
| Tuesday, December 03, 2019 | 02:30 p.m. to 05:30 p.m. | 88961 | Embedded System and RTOS |
| Thursday, December 05, 2019 | 02:30 p.m. to 05:30 p.m. | 88962 | Computer Communication Network |
| Tuesday, December 10, 2019 | 02:30 p.m. to 05:30 p.m. | 88963 | VLSI Design |
| Thursday, December 12, 2019 | 02:30 p.m. to 05:30 p.m. | 88964 | Signals and systems |
| Monday, December 16, 2019 | 02:30 p.m. to 05:30 p.m. | 88965 | Department Level Optional courses II:-Microwave Engineering |
| Monday, December 16, 2019 | 02:30 p.m. to 05:30 p.m. | 88966 | Electronics Product Design |
| Monday, December 16, 2019 | 02:30 p.m. to 05:30 p.m. | 88967 | Wireless Communication |
| Monday, December 16, 2019 | 02:30 p.m. to 05:30 p.m. | 88968 | Computer Organization and Architecture |

**(3 Hours)** **[Total Marks: 80]**

N.B : (1) Question No.1 is compulsory.

(2) Attempt any three questions from remaining questions.

(3) Figures to the right indicate full marks.

Q1) Answer any Four 20

a) What are the different Types of Tasks in a Real Time System? Give suitable Examples.

b) Differentiate between SPI and I2C Bus.

c) Give the significance of Watch Dog Timer for a given application.

d) Explain the Design Metrics of an Embedded Systems.

e) Draw the Data flow Graph for

y= $\sqrt{a^2 + b^2}$ and z = $\frac{(ab+cd)}{2}$

Q2) a) Explain the CAN Bus Protocol. How it is suitable for Real Time applications. 10

b) Explain the Task State Diagram. What is a Task Control Block.? 10

Q3) a) What is Priority Inversion, Unbounded Priority Inversion .

Give the Solution to overcome it. 10

b) Give the Utilization bound for Rate Monotonic Scheduling Algorithm

and find if the following Task Set is Ti(ei,Pi) RMA schedulable.

Show using Time Line Diagram. T1: (1,4) , T2(2,5) T3(5,20) 10

Q4) a) What type of Real Time System is a "Air Bag Deployment Unit in a Car.". 10

Write suitable PseudoCodes using MicroCOS/II functions OSInit( ), OSStart( ),

OSFlagCreate( ),OSFlagPost( )OSFlagPend( ).

Consider **Task1**:Detects Accident

**Task2**: Deploys Air bag on detection of Accident. Explain the operation of each

MicroCOS/II function used.

b) Explain the Earliest Deadline First Scheduling Algorithm. State its Advantages and Disadvantages. 10

Q5) Design a Automatic Chocolate Vending Machine.Support the Design using 20

a) Requirements b) Specifications c) Hardware /Software Architecture

e) Testing /Debugging and System Integration.

f) Use suitable MicroCOS/II functions.

Q6)Write Short Notes on **any 2** 20

a)White Box and Black Box Testing, On chip Debugging.

b)Hardware Software Co-Design Issues

c)OSTaskCreate( ),OSQPost( ),OSQPend( ),OSSemPost( ),OSSemPend( )

d)Bluetooth /Zigbee

e)Sensors and Actuators

**(3 Hours)** **[Total Marks: 80]**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions from remaining five questions.
(3) Draw neat diagrams and assume suitable data wherever necessary. Justify your assumptions.

1. Attempt any **four**: **20**
   (a) Explain the four levels of addresses used in computers.
   (b) Coaxial cable is much less susceptive to interference and cross talk than twisted pair. Why?
   (c) What is sliding window? Where is it applicable?
   (d) Explain leaky bucket to control congestion in network traffic.
   (e) Identify the class of each addresses.
   i)14.23.120.8 ii)252.5.15.111 iii)200.58.20.165 iv)128.167.23.20 v) 205.16.37.32

2. (a) Draw the OSI layer architecture. Explain the function of each layer and show the path of actual and virtual communication between the layers. **10**
   (b) What is a transparent bridge? How the process of learning in this bridge takes place. Explain the Spanning tree algorithm to solve looping problem. **10**

3. (a) Explain Persistence methods with neat diagram. **04**
   (b) Explain CSMA/CD with a flow diagram. **06**
   (c) What are the two common configurations used in HDLC? Draw and explain the HDLC frame format with separate diagram for control field format for each different frame. **10**

4. (a) Compare Stop and Wait, Selective Repeat and Go-Back-N protocols for a noisy channel **10**
   (b) Compare Circuit Switching, Packet Switching and Message Switching **10**

5. (a) List three transition strategies to move from IPV4 to IPV6. Explain the difference between tunneling and dual stack during transition period. **10**
   (b) What is Fragmentation in IPV4? Explain the fields related to fragmentation in head format. **06**
   (c) Find the first addresses, last addresses and number of addresses of the following IP addresses:- i) 205.16.37.39/28 ii) 123.56.77.29/27 **04**

6. Write Short note on **(any four)** **20**
   i) DSL
   ii) FDDI
   iii) TCP header format
   iv) Distance Vector Routing
   v) Congestion Control

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(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.

(2) Attempt any **three** questions out of **remaining five**.

(3) Assume suitable data if required.

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|---|---|---|---|
| 1. | | Solve any 4 of the following; | (20) |
| | (a) | What are the timing issues in synchronous circuit design? | (5) |
| | (b) | Implement Z= (A+B+C) D.E using CMOS gate. | (5) |
| | (c) | What is the difference between a pass transistor logic and transmission gate? | (5) |
| | (d) | Compare BJT and CMOS technology in VLSI design. | (5) |
| | (e) | How speed is improved in carry look ahead adder? | (5) |
| 2. | (a) | Explain noise margin of an nMOS inverter using VTC, critical voltages and input-output window profile. | (10) |
| | (b) | Compare SRAM and DRAM. Draw write and read circuitry of SRAM and explain its operation. | (10) |
| 3. | (a) | Implement 4*4 barrel shifter using transmission gate and explain in brief. | (10) |
| | (b) | Explain various clock skews and describe techniques to minimize it. | (10) |
| 4. | (a) | Explain CMOS inverter characteristics mentioning its all regions of operation. What is the effect of changing W/L ratio on it? Explain with example. | (10) |
| | (b) | Explain various ESD protection techniques. | (10) |
| 5 | (a) | Implement 4:1 MUX using pass transmission logic. Explain advantages of using transmission gates. | (10) |
| | (b) | Draw 1T DRAM cell and explain its write, refresh and read operation. | (10) |
| 6. | | Write short notes on any Three of the following: | (20) |
| | (a) | Switching characteristics of CMOS inverter. | |
| | (b) | Short channel effects | |
| | (c) | Importance of low power design. | |
| | (d) | ESD and its protection. | |

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**(3 Hrs)** **Total Marks: 80**

NOTE: 1) Question number 1 is compulsory.
2) Attempt any three questions from the remaining five questions.
3) Assume suitable data wherever necessary.

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Q.1 a) Prove the shifting property of Z transform. (5)

b) Distinguish between power and energy signals. Is x(t) = cos(wt) is energy or power signal? (5)

c) Check for the Dynamicity, Linearity, Time Variance, Causality and Stability $\mathbf{y(t) = e^{t\,x(t)}}$ (5)

d) Determine the Nyquist rate of the following signals $x(t) = \sin^2(200\pi\, t)$ (5)

Q.2 a) Determine the fundamental period of the following signals: (5)

(i) $x(t) = 2\cos\frac{2\pi}{3}t + 3\cos\frac{2\pi}{7}t$

(ii) $x(n) = \cos^2\{\frac{\pi}{4}n\}$

b) Find and sketch the even and odd components of the following: (5)

$x(t) = t, \quad 0 \le t \le 1$

$x(t) = 2 - t, \quad 1 \le t \le 2$

c) Obtain direct form I and II realization of a system described by (10)

$$y(n) - \frac{3}{4}y(n-1) + \frac{1}{8}y(n-2) = x(n) + \frac{1}{2}x(n-1)$$

Q.3 a) Obtain x(n) for all possible ROC conditions. Also plot the ROC comment on causality at the system. (10)

$$X(Z) = \frac{1 - 2Z^{-1}}{1 - \frac{7}{12}Z^{-1} + \frac{1}{12}Z^{-2}}$$

b) Perform the following convolution operation of two functions in time domain. $x_1(t) = u(t)$ $x_2(t) = e^{-t}u(t)$; $t \ge 0$ (10)

Q.4 a) A C.T LTI system is initially relaxed and is represented by the equation (10)

$y''(t) + 3\,y'(t) + 2\,y(t) = 2\,x(t)$

i) Determine Transfer function of the system.

ii) Determine impulse response of the system.

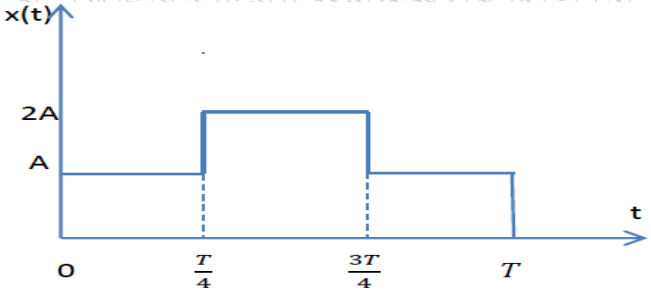
iii) Find the response of the system to an input $x(t) = 4\,e^{-3t}\,u(t)$

b) Find the response of the time invariant system with impulse response (10)

$h(n) = \{1,2,1,-1\}$ to an input signal $x(n) = \{1,2,3,1\}$

Q.5 a) Determine trigonometric form of the Fourier series of the ramp signal shown in figure. (10)


b) Obtain Fourier transform by using properties of Fourier transform only. (10)




Q.6 a) Prove Parseval's theorem of fouries series (05)

b) Determine Fourier transform of signum Signal. (05)

c) Obtain system function H(z) for (05)

$$\mathbf{y(n) + \frac{1}{2}y(n-1) = x(n) - x(n-1)}$$

Determine the poles and zeros and draw a pole zero plot.

d) Explain the causality and stability conditions for LTI systems. (05)

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**(3 Hours)** **[Total Marks: 80]**

**N.B: (1) Question No.1 is compulsory.**
**(2) Solve any three out of remaining questions.**
**(3) Assume suitable data if necessary.**

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|---|---|---|---|
| Q.1 | **Solve any Four** | | |
| | a. | What are the issues while formulating a test plan? | **05** |
| | b. | Explain the phases of new product development. | **05** |
| | c. | What are the performance and efficiency measures in hardware testing? | **05** |
| | d. | Draw and label the microstrip geometry for PCB design. | **05** |
| | e. | What is the difference between active and passive component? | **05** |
| Q.2 | a. | Explain waterfall model of software development life cycle. | **10** |
| | b. | Explain how simulation, prototyping and parametric testing support the engineering development, system integration and training. | **10** |
| Q.3 | a. | State clearly the limitations and advantages of the Spiral model in EPD. | **10** |
| | b. | Design the front panel of a digital multimeter by taking care of ergonomics and aesthetic design considerations. | **10** |
| Q.4 | a. | What are the different steps in hardware designing of an electronic product? What is the difference between system requirement specifications and design specifications? | **10** |
| | b. | What is the roll of documentation in quality product design? | **10** |
| Q.5 | a. | What is integration, verification and validation in Electronic Product Designing? | **10** |
| | b. | How to handle EMI/EMC issues in an Electronic Product? | **05** |
| | c. | What is the role of A to D converter in product designing ? | **05** |
| | **Write short note on any four** | | |
| Q.6 | a. | Need of Prototyping. | **05** |
| | b. | Image Plane. | **05** |
| | c. | Different electrical infrastructure considerations. | **05** |
| | d. | Different grounding methodologies. | **05** |
| | e. | Risk management in software testing. | **05** |

**Time: 3 hours** **Marks: 80**

N.B.
1) Question number ONE is compulsory.
2) Attempt any THREE questions from remaining questions.
3) All questions carry equal marks.
4) Figures to the right indicate full marks.

Q1
- a) What is meant by Umbrella Cell and Micro Cell in cellular systems? 5
- b) Explain authentication and security in GSM 5
- c) Differentiate between soft hand off and hard hand off 5
- d) Differentiate between CDMA, TDMA and FDMA 5

Q2 a) A total of 36 MHz of bandwidth is allocated to a particular frequency division duplex cellular telephone system, which uses two 25KHz simplex channels to provide full duplex voice and control channels. Compute the number of channels available per cell, if the system uses,
   a. 7-cell reuse and
   b. 12-cell reuse 10

b) Explain dynamic channel assignment strategy in a cellular system. What are the advantages of this scheme? 10

Q3 a) Explain with block diagram the Ground Reflection (two-ray) model of radio wave propagation. 10

b) Explain the difference between DSSS and FHSS with suitable block diagram. Which of the two is more bandwidth efficient? 10

Q4 a) Draw and explain the architecture of GSM. 10

b) Explain authentication process in a GSM system. What is the significance of white, grey and black registers ? 10

Q5 a) Explain forward and reverse channels of IS 95. 10

b) Explain UMTS network architecture in detail with interfaces 10

Q6 Write short notes on **any 2** 20
- a) GPRS
- b) Hand of procedure in GSM
- c) Erlang B and Erlang C system
- d) Wireless sensor Networks

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**Time: 3 Hrs** **Marks: 80**

1) **Question No.1 is compulsory.**
2) **Attempt any three question out of remaining five questions.**
3) **Assume suitable data whenever necessary.**

1)

a) Represent $(78)_{10}$ and $(0.6125)_{10}$ in single precision floating point. 05
b) Explain basic structure of 4 stage Pipeline. 05
c) List Different I/O Access Methods. Explain any one detail. 05
d) Differentiate between SRAM and DRAM. 05

2)

a) Explain in detail organization of Cache Coherent – Non Uniform Memory Access. 10

b) What are the different types of pipeline Hazards. 10

3)

a) Explain Restoring Division algorithm and Perform (14) ÷ (6) using it. 10

b) What is necessity of replacement algorithm? Show how pages are replaced between cache and main memory using replacement policies: 10
i) LRU
ii) FIFO
iii) LFU

4)

Explain Set Associative Mapping. Draw and explain a two-way set-associative mapping for cache that has lines of 16 bytes and a total size of 8 Kbytes. The 64-Mbyte main memory is byte addressable. 20

5)

a) What is micro programmed control? Explain in details. Write microinstruction for MOV $R_0$,[$R_1$]. 10
b) Describe Flynn's Classification for parallel computer architecture. 10

6) Write Short Notes on

a) Superscalar Architectures. 10

b) Memory segmentation 10

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