

**K. J. Somaiya Institute of Technology, Sion, Mumbai-22**  
**(Autonomous College Affiliated to University of Mumbai)**

April – May 2023

B.Tech Electronics and Telecommunication Engineering

Scheme II

Examination: SY

Semester: IV

Course Code: EXC402 and

Course Name: Microcontrollers

Date of Exam: 16/05/23

Duration: 2.5 Hours

Max. Marks: 60

Instructions:

- (1) All questions are compulsory.
- (2) Draw neat diagrams wherever applicable.
- (3) Assume suitable data, if necessary.

Q No	Statement	Max. Marks	CO	BT level
<b>Q.1</b>	<b>Solve any six questions out of eight:</b>		<b>12</b>	
i)	Outline the features of 8051.	2	1	R
ii)	What is a cache memory?	2	2	R
iii)	What is the function of $\overline{EA}$ pin in 8051?	2	3	R
iv)	What is the function of 'SWAP' instruction in 8051?	2	4	R
v)	What does 'ARM7-TDMI' represent as per the naming convention of ARM?	2	5	U
vi)	What are the application domains of Cortex A, Cortex R and Cortex M?	2	6	U
vii)	What is the function of DPTR register?	2	3	R
viii)	Explain use of 'CJNE' instruction with example.	2	4	U
<b>Q.2</b>	<b>Solve any four questions out of six.</b>		<b>16</b>	
i)	Define interrupt. What are different types of interrupts? What is interrupt priority?	4	1	U
ii)	List and explain the different types of semiconductor memory?	4	2	U
iii)	Explain Internal RAM organization of 8051	4	3	C
iv)	Explain addressing modes in 8051.	4	4	U
v)	Draw and explain ARM7 programmer's model.	4	5	U
vi)	Explain the conditional execution of instructions in ARM 7. List different conditional codes in ARM 7.	4	6	U

**K. J. Somaiya Institute of Technology, Sion, Mumbai-22**  
**(Autonomous College Affiliated to University of Mumbai)**

April – May 2023

B.Tech Electronics and Telecommunication Engineering

Examination: SY

Course Code: EXC402 and

Scheme II

Semester: IV

Course Name: Microcontrollers

Date of Exam: 16/05/2023

Duration: 2.5 Hours

Max. Marks: 60

- Q.3 Solve any two questions out of three. 16**
- i) Differentiate between
- a) RISC and CISC architecture. 8 1 U
  - b) Von-Neumann and Harvard architecture
- ii) Explain the concept of virtual memory with memory management unit, segmentation and paging. 8 2 U
- iii) Draw and explain architecture of following register. Also write significance of every bit of the register.
- a) PSW 8 3 U
  - b) PCON
  - c) TMOD
- Q.4 Solve any two questions out of three. 16**
- i) Write a program to transfer the message "HELLO" serially at baud rate of 4800, using 8-bit UART. 8 4 Ap
- ii) Explain different processor modes in ARM 7. 8 5 U
- iii) Explain what following instructions of ARM 7.
- a) ADC R3,R2,R1 8 6 U
  - b) CMN R1,R2
  - c) MLA R4,R3,R2,R1
  - d) LDR R0, [R1,#4]

\*\*\*\*\*