K. J. Somaiya Institute of [illegible] Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Subject Code: AIC304 Subject Name: Digital Logic and Computer Architecture
Date: 01/06/23

May-June: 2023
(B.Tech) Program: Artificial Intelligence and Data Science
Examination: SY Semester: III
Course Code: AIC304 and Course Name: Digital Logic and Computer Architecture
Duration: 2.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	State and prove Demoragn's theorem.	02	CO1	Ap
ii)	Perform Hex subtraction using 15's complement method. $(2AF)_{16} - (B8)_{16}$	02	CO2	Ap
iii)	Draw NAND based JK flip flop.	02	CO3	U
iv)	Identify Addressing mode of following instruction. 1) MVI AH,12H 2) ADD CL, [BX+SI]	02	CO3	R
v)	What is a hardwired control unit and state its types.	02	CO4	U
vi)	Write at least two characteristics of memory.	02	CO5	R
vii)	Perform BCD subtraction using 9's complement method. $(56)_{10} - (22)_{10}$.	02	CO2	Ap
viii)	What is Amdhal's Law?	02	CO6	U
Q.2	Solve any four questions out of six.	16		
i)	Implement XOR gate using NAND gates only.	CO1	04	Ap
ii)	Represent $(14.125)_{10}$ in single and double precision floating point numbers.	CO2	04	U
iii)	Implement Full Adder using half adder.	CO3	04	U
iv)	Compare RISC and CISC architecture.	CO4	04	U
v)	Explain Memory Hierarchy with suitable diagrams.	CO5	04	U

vi)	State types of pipeline hazards.Explain at least one in detail.	CO6	04	U
Q.3	Solve any two questions out of three.	16		
i)	Find BCD code, Excess-3 code and Gray code of given number i)$(214)_{10}$ ii)$(349)_{10}$	8	CO1	Ap
ii)	What is a Microprogrammed control unit? Compare horizontal and vertical Microprogrammed control units	8	CO1	U
iii)	Consider a 4 way set associative memory mapping cache of size 8KB with block size of 32 bytes. The size of Main memory is 4 GB Find 1. No. of sets in main memory 2. No. of lines in cache. 3. No.of bits in tag 4. Represent physical address Show Memory mapping with the help of a suitable diagram. Also comments on the number of searches in 4 way set associative memory mapping.	8	CO4	Ap
Q.4	Solve any two questions out of three.	16		
i)	Perform -7 X -3 multiplication using booth's algorithm.	08	CO2	Ap
ii)	Design 3 bit Asynchronous counter.	08	CO3	Ap
iii)	Consider a pipeline having 4 phases with duration 150,120,160 and 140 ns. Given latch delay is 5ns. Calculate - Pipeline cycle time, Non pipeline execution time, Speed up ratio, pipeline time for 1000 tasks, Efficiency and throughput.	CO6	8	Ap

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