K. J. Somaiya Institute of ~~Engineering and Information~~ Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Subject Code: CEC304   Subject Name: Digital Logic & Computer Architecture   Date: 01/06/23

May-June 2022-23
(B.Tech) Program: Computer Engineering
Examination: SY Semester: III
Course Code: CEC304   and   Course Name: Digital Logic & Computer Architecture

Duration: 2.5 Hours   Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	Describe the different types of Read Only Memory (ROM).	2	CO5	U
ii)	Convert $(314)_8$ to binary and decimal.	2	CO1	Ap
iii)	Explain superscalar processor.	2	CO6	U
iv)	Subtract using 2's complement $(9)_{10} - (5)_{10}$.	2	CO2	Ap
v)	Explain IEEE 754 standard floating point number representation.	2	CO2	U
vi)	Describe Demultiplexer in detail.	2	CO3	U
vii)	Explain the concept of microinstruction.	2	CO4	U
viii)	Describe binary and octal number system.	2	CO1	U
Q.2	Solve any four questions out of six	16		
i)	Explain universal gates with truth table and logic diagram.	4	CO1	Ap
ii)	Compare hardwired and micro-programmed control unit.	4	CO4	U
iii)	Explain six stage pipelining for instruction execution.	4	CO6	U
iv)	Draw and explain flowchart for restoring division algorithm for unsigned integer.	4	CO2	U
v)	Explain the instruction cycle in details.	4	CO3	U
vi)	Explain direct memory mapping technique.	4	CO5	U
Q.3	Solve any two questions out of three.	16		

K. J. Somaiya Institute of Engineering and Information Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Subject Code: CEC304   Subject Name: Digital Logic & Computer Architecture   Date: 01/06/23

i)	Explain Von Neumann and Harvard Architecture in detail.	8	CO1	U
ii)	Implement full adder circuit with logic diagram and Boolean expression.	8	CO3	Ap
iii)	Multiply (-9) and (7) using Booth's Algorithm.	8	CO2	Ap
Q.4	Solve any two questions out of three.	16		
i)	Explain different technique for Hardwired Control Unit using state table and delay element method.	8	CO4	U
ii)	Explain SRAM and DRAM memory cell with diagram.	8	CO5	U
iii)	Discuss various pipeline hazards.	8	CO6	U

****