

K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

April – May 2023

B.Tech Electronics and Telecommunication Engineering
Examination: SY
Course Code: 1UEXC402 and

Scheme **I**
Semester: IV
Course Name: Microcontrollers

Date of Exam: 27/05/23

Duration: 2.5 Hours

Max. Marks: 60

Instructions:

- (1) All questions are compulsory.
- (2) Draw neat diagrams wherever applicable.
- (3) Assume suitable data, if necessary.

Q No	Statement	Max. Marks	CO	BT level
Q.1	Solve any six questions out of eight:		12	
i)	Explain Three Bus Architecture, and brief about T-State.	2	1	R
ii)	Explain different types of Semiconductor memories	2	2	R
iii)	Explain the function of ALE and EA' pins in 8051.	2	3	R
v)	List 8051 Data types and directives	2	4	R
v)	What does 'ARM7-TDMI' represent as per the naming convention of ARM?	2	5	U
vii)	Distinguish between Thumb state and ARM state	2	5	R
vii)	List PORT 3 alternate functions in 8051.	2	3	R
viii)	Explain use of 'RRA' and 'RLC' instruction with example.	2	4	U
Q.2	Solve any four questions out of six.		16	
i)	Define interrupt. What are different types of interrupts? What is interrupt priority?	4	1	U
ii)	Classify Memory : Primary and Secondary	4	2	R
iv)	What do you understand by addressing modes? List addressing modes supported by 8051 with one example of each.	4	3	R
iv)	Explain Stack and Stack pointer in brief with examples	4	4	U
v)	Explain the following instruction related to ARM 1) ADD r0,r1,r1,LSL #2 2) LDR r0,[r1],#4	4	5	R
vi)	Explain the concept of Pulse-Width Modulator Configuration in ARM 7.	4	6	R

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Scheme II

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Q.3	Solve any two questions out of three.				16
i)	Draw and explain Architecture of 8051.	8	1	R	
ii)	WAP to find smallest in series using ARM 7.	8	6	Ap	
iii)	Explain ARM 7 operating modes.	8	5	R	
Q.4	Solve any two questions out of three.				16
i)	Write an ALP to find the largest number in series using 8051.	8	4	Ap	
ii)	Write an ALP to generate a square wave of 2KHz at P 2.3. Use timer 1 in model.	8	3	Ap	
iii)	Explain Virtual Memory Concept with Memory Management Unit with Segmentation and Paging.	8	2	R	
