K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
August 2023
(B.Tech) Program: EXTC Scheme I/II: II
Examination: **Supplementary Exam** TY Semester: V
Course Code: **EXC502** and Course Name: **Digital VLSI Design**

Date of Exam: 8th August 23 Duration: 2.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	What is photolithography?	2	1	R
ii)	Define rise time for CMOS inverter	2	2	R
iii)	Realize y=/(AB+CD) using static CMOS design style.	2	3	A
iv)	List different types of semiconductor memories.	2	4	R
v)	Draw Human Body Model (HBM) for Electrostatic Discharge (ESD).	2	5	R
vi)	List the steps involved in RTL design.	2	6	R
vii)	Draw 2:1 mux using transmission gate.	2	3	A
viii)	Draw 4 bit ripple carry adder block diagram. Find the total delay if delay of individual stage is 2ns.	2	5	A
Q.2	**Solve any four questions out of six.**	**16**		
i)	Write short note on MOSFET scaling.	4	1	R
ii)	Draw circuit diagram and stick diagram for CMOS inverter.	4	2	A
iii)	Draw following circuits using C^2MOS design style. a) NAND gate b) NOR gate	4	3	A
iv)	Design a NAND ROM to save the given binary data: 0110, 1010, 0001, 1011	4	4	A
v)	Demonstrate addition of $(1101\ 1000\ 0101\ 1110)_2$ and $(0011\ 1001\ 0010\ 0001)_2$ using carry select adder.	4	5	A
vi)	Design a datapath of parallel 3 tap FIR filter using RTL design.	4	6	C

Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain all steps involved in the fabrication of NMOS with proper diagram.	8	1	R
ii)	Draw and explain Voltage Transfer Characteristics for CMOS inverter.	8	2	R
iii)	Draw 3T-DRAM cell. Explain read '0', write '0', read '1' and write '1' operation.	8	4	U
Q.4	**Solve any two questions out of three.**	**16**		
i)	Realize 8:1 using transmission gate.	8	3	A
ii)	Draw 4 bit array multiplier. Highlight the worst case delay path. Find out the worst case delay if propagation delay of the components is as follows: AND gate: 1ns Half Adder: 2ns Full Adder: 2ns	8	5	A
iii)	Design Soda Dispenser machine using RTL design. Implement HLSM, Datapath and FSM.	8	6	C

****