K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

Feb/March 2024

(B.Tech) Program: Artificial Intelligence and Data Science Scheme I/II/IIB/III: IIB
Examination: SY Semester: III
Course Code: AIC304 and Course Name: Digital Logic and Computer Architecture

Date of Exam: 01/03/24 Duration: 2.5 Hours Max. Marks: 60

Supplementary Examination

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Max. Marks	CO	BT level
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Convert Binary to decimal, octal, Hex (Use standard method and show all the steps) $(1101010011)_2$	2	CO1	Ap
ii)	What are weighted and non-weighted codes? Explain with examples.	2	CO1	U
iii)	Obtain 1's complement and 2's complement of given number. $(1011)_2$	2	CO2	Ap
iv)	Draw Half Adder using NOR gates only	2	CO3	U
v)	Explain microinstruction format.	2	CO4	U
vi)	What is Locality of reference and its types.	2	CO5	U
vii)	What is Amdahl's law?	2	CO6	U
viii)	What is bus contention and arbitration?	2	CO6	U
Q.2	**Solve any four questions out of six.**	**16**		
i)	Implement given logic gate/Boolean expression using NAND gates only. $(A+B+C) \cdot (A' + C')$	4	CO1	Ap
ii)	Perform Binary subtraction using 2's complement number. $(-8) - (5)$	4	CO2	Ap
iii)	Derive T flip flop from JK flip flop	4	CO3	Ap
iv)	Compare RISC and CISC architecture.	4	CO4	U
v)	Draw and Explain Memory Hierarchy	4	CO5	U
vi)	Explain control hazards with suitable examples.	4	CO6	U

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Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain Von-Neumann's architecture in detail.	08	CO1	U
ii)	What is a Microprogram? Write microprogram for following instructions 1) MOV A,B 2) ADD A,M	08	CO4	U
iii)	Consider a 2 way set associative mapped cache of size 32 KB with block size 512 bytes. The size of the main memory is 256 KB. Find- 1. Number of bits in tag 2. No. of sets in main memory. 3. No. of bits in a set. 4. Word size. How many bits are required to represent a memory physical address shown with format.	08	CO5	Ap
Q.4	**Solve any two questions out of three.**	**16**		
i)	Perform Multiplication of the following numbers using Booth's Algorithm. (-4) * (-6)	08	CO2	Ap
ii)	Draw and explain Instruction cycle state diagram with and without interrupt handling.	08	CO3	U
iii)	With the following parameters draw a phase timing diagram and find speed up factor and efficiency for 5 stage pipelining. Number of instructions =10 and processor frequency 5 MHz., data and branch hazards that occur in the computer system.	08	CO6	AP

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