DECEMBER-2019

EXAMINATION TIME TABLE
T.E.(ELECTRONICS)(Sem VI) (CBSGS)

Days and Dates	Time	Paper Code	Paper
Tuesday, December 03, 2019	02:30 p.m. to 05:30 p.m.	37201	BASIC VLSI DESIGN
Thursday, December 05, 2019	02:30 p.m. to 05:30 p.m.	37202	ADVANCED INSTRUMENTATION SYSTEM
Tuesday, December 10, 2019	02:30 p.m. to 05:30 p.m.	37203	COMPUTER ORGANIZATION
Thursday, December 12, 2019	02:30 p.m. to 05:30 p.m.	37204	POWER ELECTRONICS - I
Monday, December 16, 2019	02:30 p.m. to 05:30 p.m.	37205	DIGITAL SIGNAL PROCESSING AND PROCESSORS
Wednesday, December 18, 2019	02:30 p.m. to 04:30 p.m.	37206	MODERN INFORMATION TECHNOLOGY FOR MANAGEMENT

(3 Hours) **[Total Marks: 80]**

Note: 1.Question 1 is compulsory.
2.Solve any three out of remaining .
3.Assume suitable data if necessary
4.Draw proper diagrams

Q.1. Solve any four.

(a) Compare Biploar,NMOS and CMOS technologies (min three points) . **[05]**

(b) Design a 2:1 MUX using transmission gates and discuss advantages of use of transmission gate logic. **[05]**

(c) Implement $Y=\overline{(A.B)+(C.D)}$ using Dynamic Logic. **[05]**

(d) Compare Ram and ROM. **[05]**

(e) Explain clock generation techniques. **[05]**

Q.2 (a) Sketch and explain the general shape of the Transfer characteristics of NMOS inverter.Compare different types of inverters. **[10]**

(b) Compare the full scaling model with constant voltage scaling model for MOSFETS. Demonstrate clearly the effects of scaling on the device density, speed of the circuit, power consumption and current density of the gates. **[10]**

Q.3 (a) Implement D flip-flop using Static CMOS. What are other design methods for it?

(b) Explain READ and WRITE operation of 6-T SRAM cell in detail. **[10]**

Q.4 (a) What is ESD protection? Explain with example. **[10]**

(b) Explain Carry Look Ahead adder and it's advantages. **[10]**

Q.5 (a) What are different clock distribution schemes? Explain concept of Global and Local clock. **[10]**

(b) What are various decoders used in memory structures? Explain any one in detail. **[10]**

Q.6. Write short notes on **(any three)** **[20]**

(a) NORA ,Zipper Logic design
(b) Flash Memory
(c) CMOS latch-up and its prevention
(d) Sense Amplifier

(Time: 3 Hours) **Total Marks: 80**

Note: 1) Question No.1 is compulsory.
2) Attempt any three questions from remaining five questions.
3) Assume suitable data if necessary.
4) Figures to the right indicate full marks.

Q.1) Explain in brief

a) Data logger 5M

b) Proportional controller 5M

c) Pneumatic logic gates 5M

d) DP transmitter 5M

Q.2) a) Give the classification of compressors. Explain any two rotary compressors with diagram. 10M

b) Explain flapper nozzle system. Explain any two applications of flapper nozzle system for industrial use. 10M

Q.3) a) What are the different types of contol valve actuators? Explain the working of an elecro-mechanical actuator. 10M

b) What are the different types of hydraulic pumps? Explain with neat sketch. 10M

Q.4) a) What is the necessity of controller tuning? Explain different methods of controller tuning with required sketches. 10M

b) Explain the detail construction cylinder with its dynamics. 10M

Q.5) a) Draw the diagram of telemetry and explain the working in detail. 10M

b) Explain compressed air receiver unit. What are the different control strategies for air receiver unit? 10M

Q.6) a) Compare electronic versus pneumatic transmitters. Explain the 2 wire and 3 wire transmitter. 10M

b) Explain the terms rangeability and control valve sizing. A velocity control system has a range of 200 mm/s to 480 mm/s. If the set point is 327 mm/s and the measured value is 294 mm/s, calculate the error as % of span. 10M

(3 Hours) **(Total Marks : 80)**

N.B.: 1) **Question No.1** is **compulsory**.
2) Attempt **any three** questions from remaining questions.
3) **Figures** to the **right** indicate **full marks**.

Q1.	(a)	Explain IEEE 754 format for 32 bit numbers	**5**
	(b)	How does cache memory improve system performance?	**5**
	(c)	Write short notes on nano programming	**5**
	(d)	Write short notes on memory hierarchy	**5**
Q2.	(a)	Explain Booth's algorithm. Solve 6*5 using Booth's algorithm. 5 is multiplier	**10**
	(b)	Draw the flowchart for restoring division algorithm. Solve 9 ÷ 4 using restoring division algorithm	**10**
Q3.	(a)	What is microprogramming? Draw and explain microprogrammed control unit	**10**
	(b)	Explain hardwired control unit with a neat diagram. Describe clearly the generation of control signals with examples	**10**
Q4.	(a)	Explain the paging mechanism. State advantages of paging and the importance of the translation lookaside buffer (TLB) in paging.	**10**
	(b)	Consider a 2-way set associative mapping with block size =16 bytes, cache size=16k main memory size =256k. Design a cache structure and show how the processor address is interpreted..	**10**
Q5.	(a)	State the advantages of pipelining. Explain any two types of pipeline hazards and their solutions.	**10**
	(b)	What is the necessity of a replacement algorithm? Explain how pages are replaced using LRU and LFU algorithms	**10**
Q6.	(a)	Briefly explain programmed I/O, interrupt driven I/O and DMA	**10**
	(b)	Explain with examples any five addressing modes of IA32 processors	**10**

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(3Hours) **[Total Marks:80]**

N.B.: (1) Question No. 1 is compulsory.
(2) Solve any three questions out of remaining five questions.
(3) Figures to the right indicate full marks.
(4) Assume suitable data if required.

1. Attempt the following :- **20**
   (a) Draw and explain the static V-I characteristics of SCR. Define the latching and holding current.
   (b) Explain the principle of operation of single phase voltage controller with R load.
   (c) What is pulse width modulation? List the various PWM techniques. How do these differ from each other?
   (d) Explain the principle of operation of Dual Converter.

2. (a) Explain with neat circuit diagram and waveforms the operation of three phase half controlled rectifier with R load. **10**
   (b) With the help of neat diagram, explain the operation of R-C firing circuit. Also draw and explain the associated waveforms. **10**

3. (a) Explain the operation of single phase, fully controlled bridge converter with RL load. Derive the expression for average load voltage and load current. **10**
   (b) With the help of neat diagram and associated waveforms discuss the operation of Buck-Boost converter. **10**

4. (a) Explain with neat diagram and waveform the operation of single phase half bridge voltage source inverter with R-L load. **10**
   (b) Draw and explain the output characteristics of n-channel MOSFET. What is the significance of the safe operating area of a power MOSFET? **10**

5. (a) Explain the working of single phase cyclo converter with the help of neat diagram and waveforms. **10**
   (b) Explain the working of three phase bridge inverter in 180° conduction mode with circuit diagram and associated waveform. **10**

6. (a) Why commutation is required in thyristor circuits? State various commutation techniques used for thyristors. Describe class 'C' commutation with relevant waveforms. **10**
   (b) With the help of neat structural diagram, explain the operation of GTO. Also explain its switching behaviour. **10**

Duration 3 Hours **[Maximum marks 80]**

NOTE:-1) Question 1 is **compulsory**
2) Solve **any three** from the remaining five questions
3) Assume suitable data if necessary.
4) Figures to the right indicate full marks

Q.1. a. State and explain relation between L.T and Z.T **20**

b. What are special features of DSP Processor?

c. Compare BLT and ILT.

d. What do you mean limit cycle oscillations?

Q.2. a. Explain different windowing techniques in FIR filter design **10**

b. Explain Gibb's phenomenon and it's physical interpretation in filter design. **10**

Q.3. a. Given the transfer function of the analog filter $(\boldsymbol{s}) = \frac{\mathbf{1}}{(\boldsymbol{S}+\mathbf{1})(\boldsymbol{S}+\mathbf{3})}$, **10**

T= 2 second. Design IIR filter using BLT method. Explain the concept of frequency warping.

b. Explain product quantization error with suitable example. **10**

Q.4. a. Explain the architecture of TMS32067xx DSP processor. **10**

b. Explain different addressing modes of DSP processor. **10**

Q.5. a. Compute the 8-point DFT of the sequence using DIT-FFT algorithm **10**

$\boldsymbol{x(n)} = \{\mathbf{0.5}, \mathbf{0.5}, \mathbf{0.5}, \mathbf{0.5}, \mathbf{0}, \mathbf{0}, \mathbf{0}, \mathbf{0}\}$

b. Find the linear convolution of the sequences **10**

$\boldsymbol{x(n)} = \{\mathbf{1}, \mathbf{2}, \mathbf{3}, \mathbf{4}\}$ and $\boldsymbol{h(n)} = \{\mathbf{1}, \mathbf{1}, \mathbf{1}\}$.

Also obtain the same result using circular convolution.

Q.6. a. Explain the significance of VLIW architecture in DSP processor. **10**

b. Explain the application of DSP in speech processing. **10**

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(2 Hours) **[Total Marks: 40]**

N.B. **(1) Question No. 1** is **compulsory**.
(2) Attempt **any three** questions from remaining **five**.
(3) Each question carries **10** marks.

1. Answer **any five** of the following:
   a. Which are the components of IT Infra? 2
   b. What is data mining? 2
   c. Differentiate between DBMS and RDBMS. 2
   d. Illustrate the four layered reference model for TCP/IP. 2
   e. Explain any four top security concerns. 2
   f. Explain E-governance framework. 2
   g. Explain CIA triangle in brief. 2

2.
   a. Define Cabling. Classify cable types and explain in detail. 5
   b. Define topology. Explain any 3 common topologies. 5

3.
   a. Explain following IP Addressing Mechanism 5
      i. IP V4-Address System
      ii. IPV6 Address system
      iii. User Datagram Protocol
   b. Write detailed note on SNMP. 5

4. Write a note on following terms related to IT audit. 10
   a. Information Audit.
   b. Audit Schedule.
   c. Audit Plan.
   d. Audit Preparation.
   e. Internal Audit.

5.
   a. Illustrate Enterprise Resource Planning (ERP) and its need in detail. 5
   b. Write a note on E-Commerce 5

6. Write short notes on **any two** of the following : 10
   a. Firewall.
   b. RFID systems.
   c. Biometric systems.
   d. IP-CCTV.
   e. End point security.

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