

K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

May – June 2024		
(B. Tech) Program: Electronics and Telecommunication Engineering		
Scheme II		
Regular Examination: SY Semester: IV		
Course Code: EXC403 and Course Name: Linear Integrated Circuit		
Date of Exam: 18/05/24	Duration: 2.5 Hours	Max. Marks: 60

Instructions:				
(1) All questions are compulsory.				
(2) Draw neat diagrams wherever applicable.				
(3) Assume suitable data, if necessary.				
		Max. Marks	CO	BT level
Q 1	Solve any six questions out of eight:	12		
i)	Draw block diagram of operation amplifier.	2	1	U
ii)	Draw circuit diagram of practical Integrator.	2	2	U
iii)	Write formula for UTP and LTP for inverting Schmitt Trigger.	2	3	R
iv)	Draw Pin Configuration of IC 555.	2	4	U
v)	Draw Circuit of HVLC IC 723.	2	5	R
vi)	Define lock range.	2	6	R
vii)	Draw Circuit diagram of band reject filter.	2	2	U
viii)	Draw Circuit diagram of precision half wave rectifier.	2	3	U
Q.2	Solve any four questions out of six.	16		
i)	Explain concept of virtual ground and virtual short with the help of diagram,	4	1	U
ii)	Mention requirement of instrumentation amplifier.	4	2	U
iii)	Compare Zero Crossing detector and Schmitt trigger.	4	3	U
iv)	With a neat circuit diagram. Explain the working of PWM using IC 555.	4	4	U

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V)	Design 1A current source using IC 7805. assume $R_L = 10 \text{ ohm}$.	4	5	A
Vi)	Write Features of 566 VCO IC.	4	6	U
Q.3	Solve any two questions out of three.	16		
i)	<p>eg) Find V_o for adder-subtractor ckt shown below</p>	8	1	A
ii)	Design the Astable Multivibrator using IC555 to provide output square wave with frequency of 1 KHz, for duty cycle of 60%.	8	4	A
iii)	Explain Switching regulator with block diagram in details.	8	5	R
Q.4	Solve any two questions out of three.	16		
i)	Design 1 st order HPF for cut off frequency of 6 KHZ and pass band gain of 2.	8	2	A
ii)	Design a triangular wave generator so that $F_o = 2 \text{ KHZ}$, & $V_o \text{ pp} = 7 \text{ V}$. The op amp is operating @ $\pm 15 \text{ V}$.	8	3	A
iii)	Draw and explain PLL block in details with its IC configuration.	8	6	U
