DECEMBER-2019

EXAMINATION TIMETABLE
T.E.(ELECTRONICS & TELE-COMMN.)(Sem VI) (CBSGS)

Days and Dates	Time	Paper Code	Paper
Tuesday, December 03, 2019	02:30 a.m. to 05:30 p.m.	37001	DIGITAL COMMUNICATION
Thursday, December 05, 2019	02:30 a.m. to 05:30 p.m.	37002	DISCRETE TIME SIGNAL PROCESSING
Tuesday, December 10, 2019	02:30 a.m. to 05:30 p.m.	37003	COMPUTER COMMUNICATION AND TELECOM NETWORKS
Thursday, December 12, 2019	02:30 a.m. to 05:30 p.m.	37004	TELEVISION ENGINEERING
Monday, December 16, 2019	02:30 a.m. to 05:30 p.m.	37005	OPERATING SYSTEMS
Wednesday, December 18, 2019	02:30 a.m. to 05:30 p.m.	37006	VLSI DESIGN

Duration: 3 Hrs Total Marks: 80

N.B: Question No 1 is compulsory.
Attempt any three questions out of remaining five**.**
All questions carry **equal** marks
Assume Suitable data, if required and state it clearly.

Q1) (20)

a) State and explain Shannon-Hartley theorem.
b) What is the cause of Inter Symbol Interference (ISI)
c) Explain the need of continuous wave modulation in detail.
d) Explain in brief with block diagram Integrate and Dump receiver.
e) List advantages and limitations of spread spectrum system.

Q2) a) Consider the seven symbols of Discrete Memoryless Source and their probabilities as shown in the table below. Follow the Huffman's algorithm to find the code words for each message. Also find the average code word length and the average information per message. (10)

Message	M_1	M_2	M_3	M_4	M_5	M_6	M_7
Probabilities	0.25	0.25	0.125	0.125	0.125	0.0625	0.0625

b) Derive the expression for minimum probability of error for matched filter. (10)

Q3) a) Explain the different line codes used for data transmission. (10)
b) Draw and explain the block diagram of OQPSK transmitter and receiver. Also draw the signal space representation. (10)

Q4) a) With relevant expressions and block diagram explain BFSK transmitter and receiver. Compare BPSK and BFSK. (10)

b) Consider a (7, 4) liner block code whose parity check matrix is (10)

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}$$

Obtain Generator matrix and calculate the syndrome vector for single bit error.

Q5) a) Design feedback shift register encoder of (8, 5) cyclic code for the generator polynomial $g(x) = 1+X+X^2+X^3$.Use this encoder to find code word in systematic form for the message (11001). (10)

b) Define the following: (10)

i. Systematic and non-systematic codes.
ii. Hamming weight.
iii. Hamming distance.
iv. Rate of code.
v. Properties of Hamming code.

Q6) a) Draw and explain the block diagram of DSSS transmitter and receiver with coherent BPSK. Also draw relevant waveforms at various stages of the block diagram (10)

b) Draw the block diagram of MSK transmitter .Explain why MSK is called shaped QPSK. (10)

(3 Hours) **[Total Marks: 80]**

N.B.: (1) **Questions No.1** is **compulsory**.
(2) Attempt **any three** questions out of remaining **five** questions.
(3) Assume suitable **data** if **required**.
(4) **Figures** to the **right** indicate **full marks**.

Q 1.Solve **any four** **20**

a) What method would you adopt to filter long data sequence? Explain any one method.
b) Given an analog filter, you are directed to design a digital IIR filter with the same specifications, list the steps you would follow. How would you go about the task and what desirable properties of the conversion techniques would you cite?
c) List the application of multirate signal processing. Explain the importance of multirate digital signal processing.
d) How does the position (within or outside of unit circle) of the zeros effect the phase of the system?
e) Retrieve the original sequence *x(n)* from *X(k)*=[2, 1-j, 0, 1+j] using IDIF-FFT only.

Q2 a) Determine the N-point DFT, using DIT-FFT only, of the signal **10**

$$x(n) = 6cos^2\left(\frac{n\pi}{4}\right) for\ 0 \le n \le 7$$

b) Design a High pass filter that is monotonic in pass-band with cut-off frequency of 1000 Hz and down 10 dB at 350 Hz, using Bilinear Transform, with f_s=5000 Hz. **10**

Q3 a) Compute the DFT of 2- 4 point sequences p(n)= [2 1 5 4] and q(n)=[4 6 3 2] using 4 point DFT only once. **10**
b) Explain with suitable examples how zeros are positioned under different symmetry conditions of a linear phase FIR filter. **10**

Q4 a) Design a Chebyshev filter for the given specifications using impulse invariance technique **10**

$$0.8 \le \left|H\left(e^{jw}\right)\right| \le 1 \quad 0 \le \omega \le 0.2\pi$$
$$\left|H\left(e^{jw}\right)\right| \le 0.2 \quad 0.6\pi \le \omega \le \pi$$

b) Design a high pass filter with frequency response using Hanning window of N=11. **10**

$$H_d\left(e^{jw}\right) = 1\ for\ \frac{-\pi}{4} \le \omega \le \pi$$
$$= 0\ for \qquad |\omega| \le \frac{\pi}{4}$$

Q5 a) Find DFT of a 4-point sequence *x(n)*=[1, 2, 3, 4], then using properties of DFT find the DFT of $x_1(n)$=[1, 0, 2, 0, 3, 0, 4, 0] and $x_2(n)$= [1, 2, 3, 4, 1, 2, 3, 4]. **10**
b) Explain the Finite length effects in Digital Filters. **10**

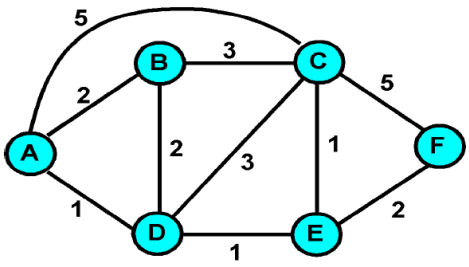
Q6 a) Explain DTMF application of digital signal processing. **10**
b) Explain sub-band coding of speech signal with neat illustration. **10**

Duration: 3 hours **Max marks: 80**

Note the following instructions.

(a) Question No.1 is compulsory(attempt any 4)
(b) Total 4 questions need to be solved
(c) Attempt any three questions from remaining five questions.
(d) Assume suitable data wherever necessary, justify the same

1.a	What is framing? How frames can be classified?	[5]
1.b	A pure ALOHA network transmits 200 bit frames on a shared channel of 200 kbps. What is the throughput if the system (all stations together) produces: (i) 1000 frames per second (ii) 500 frames per second (iii) 250 frames per second	[5]
1.c	Explain Three-Way Handshaking for connection establishment in TCP	[5]
1.d	What is the subnetwork address if the destination address is 200.45.34.56 and the subnet mask is 255.255.240.0?	[5]
1.e	Differentiate between Bus Topology and Ring Topology	[5]
2.a	Explain OSI model. Consider a source, destination machine and some intermediate nodes for the discussion.	[10]
2.b	i. Differentiate between TDM and FDM ii. Explain various addresses used in TCP/IP Layered Architecture.	[10]
3.a	What is DSL Technology? List different DSLs available. Discuss salient features of ADSL	[10]
3.b	Explain CSMA/CD in detail and also mention its use	[10]
4.a	Draw and explain TCP Header format.	[10]
4.b	What is sliding window protocol? Explain Stop and Wait ARQ in detail.	[10]
5.a	a) Using the below figure, apply the Bellman-Ford algorithm to find both the minimum cost from each node to the destination node (assume node F) and the next node along the shortest path. Also draw the tree diagram.	[10]



5.b	Define Classful addressing scheme used in IPV4. What is a mask and range of addresses used for each class?	[10]
6	Write short notes on any two. 1. HFC 2. ATM 3. DNS	[20]

(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No. 1 is compulsory.
(2) Answer any Three out of remaining five questions.
(3) Draw the neat diagrams wherever necessary.

1. (a) Explain active and passive matrix of LCD. 05
(b)In TV why AM is preferred over FM for picture modulation. 05
(c)Explain when and why the horizontal sweep oscillator step out of synchronism. 05
(d) What is the need of MUSE system. 05

2. (a) Draw and explain Horizontal sync details compared to horizontal deflection saw tooth wave. 10
(b) Explain D2-MAC packet format for sound/Data signal. 10

3. (a) Why are serrations needed in vertical sync pulses and how it solves the problem of half-line discrepancy? Explain with diagram. 10

(b) Draw and explain Image orthicon camera tube. What is the function of the electron multiplier section? 10

4. (a) Draw and explain NTSC decoder along with the explanation for Phasor diagrams of the signals in the NTSC system. 10
(b) In relation to digital TV discuss?
- Digitization,
- pixel array,
- scanning notation,
- viewing distance and angle,
- aspect ratio,
- frame rate and refresh rate. 10

5.(a)Explain with diagram wide dimension HDTV. 10
(b) What is the difference between component video and composite video? Give the main features of CCIR Rec.601for digital video standards. 10

6. Write short notes on (any two): ---
(a) EBU MAC system. 20
(b) VSB Transmission for TV, how much frequency is allocated for attenuation slope and why?
(c) Sync pulse separation and generation of vertical and horizontal sync pulses.

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(3 Hours) **[Total Marks: 80]**

N.B.: (1) Question No.1 is **compulsory.**
(2) Solve any **three** from remaining **five** questions.
(3) Assume Suitable Data if required.

Q1 Attempt any **Four.** 20
(a) What is a system call? Di:;cuss various system calls in short 05
(b) What is PCB? Explain various fields of PCB. 05
(c) Compare Paging and Segmentation scheme used in Memory management. 05
(d) What is a Kernal? Compare Micro and Monolithic Kernel. 05
(e) What are the different features ofRTOS? 05
(t) Compare and Contrast: thread and process. 05

Q2 (a) What is process? Explain the life cycle of a process using process state transition diagram. 10
(b) What is critical section problem? What is the solution to the critical section. 10

Q3 (a) schedulers 10
(b) What is a directory system? What are the different types of directory structure? 10

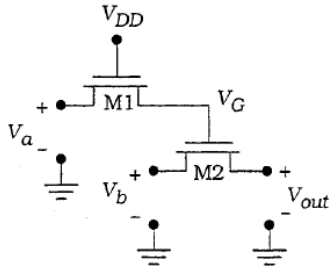
Q4 (a) Suppose that a disk drive has 5000 cylinders, numbered 0 to 4999. The drive is currently serving a request at cylinder 143, and the previous request was at cylinder 125. The queue of pending requests, in FIFO order is
86,1470,913,1774,948,1509,1022,1750,130
Starting from the current head position, what is the total distance (in cylinders) that the disk arm moves to satisfy all the pending requests for each of the following dis-scheduling algorithms?
a. FCFS
b. SSTF
c. SCAN
d. LOOK
e. C-SCAN (change data)
(b) Explain working of EDF and RMA real time scheduling algorithms. Differentiate between Deadlock A voidance and Deadlock prevention. 10

Q5 Write a note on **(any 2)** 20
a) Cyclic Schedulers
b) I-Node structure
c) File Allocation methods
d) Demand Paging

Time: 3 Hours **Marks: 80**

N.B: (1) Question No 1 is compulsory. Solve any three from the remaining five questions
(2) Figures to right indicate full marks
(3) Assume suitable data if necessary and mention the same in the answer sheet

1. Solve the following 20M
   a. Implement 4:1 Mux using Transmission Gate.
   b. Explain charge sharing in detail with proper diagram
   c. Explain different CMOS clock generation methods
   d. For following circuit diagram Vdd = 3.3V, Vt =0.6 V Find Vout for
      1) Va = Vb = 3.3 V and (2) Va = 0.5 V Vb = 3 V



   e. Draw 6T SRAM cell

2A. Explain the process of nMOS fabrication with the help of neat sketches along with the masks required 10M

2B. Draw 4x4 bit NOR based ROM array to store the following data in respective memory locations 10M

Memory Address	Data
0001	0011
0010	1101
0100	0110
1000	1101

3A. Implement $Y = \overline{(k + lm)np}$ using any 4 of the following design styles 10M
   I. Dynamic pMOS array
   II. Dynamic nMOS Array
   III. Domino Gate
   IV. Static CMOS
   V. Pseudo nMOS

3B. Implement CMOS Clocked JK latch and draw layout using lambda rules 10M

4A. Consider CMOS inverter circuit with following parameters $V_{dd} = 3.3V$, $k_r = 2.5$, $k_n = \frac{200\mu A}{V^2}$, $k_p = \frac{80\,\mu A}{V^2}$, $V_{T0n} = 0.6V$, $V_{T0p} = -0.7V$ calculate the critical voltages $V_{OL}, V_{OH}, V_{IL,} V_{IH}$ and the noise margin of the circuit. Note inverter is not symmetric. 10M

4B. For CMOS inverter derive VIL,VOH,VIH and VOL. also Find Noise margin 10M

5A. Draw circuits for the following using CMOS 10M

i. Carry Circuit of 4-Bit CLA adder using Dynamic NMOS

ii. 1-BIT Full adder (Hint - 28 transistors circuits)

5B. Draw and explain 4-bit carry save multiplier with neat diagram 10M

6A. Draw the CMOS circuit for $Y = \overline{A + DE + F}$ and find an equivalent CMOS inverter circuit for simultaneous switching of all inputs, assuming that *(W/L)* = 10 for all pMOS transistors and *(W/L)* = 15 for all nMOS transistors. 10M

6B. Write brief notes on any 2 of the following 10M

I. Clocking methods

II. Clock distribution

III. Short channel effects