K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

May-2024

Program: **B.Tech** | Scheme: **II**
Regular Examination: **LY** | Semester: **VIII**
Course Code: **EXDLC8023** | Course Name: **System On Chip**
Date of Exam: **16/05/24** | Duration: **02.5 Hours** | Max. Marks: **60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		M	CO	BT
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Draw a block diagram of a typical SOC showing the constituents blocks.	2	1	R
ii)	What are architectural and implementation challenges in SoC system design	2	2	U
iii)	Write RTL code for 2:1 MUX using dataflow design style.	2	3	A
iv)	What is a self-checking testbench?	2	4	U
v)	What is floor-planning in SoC physical design?	2	5	U
vi)	Define following terms related to physical design of SoC: a) Routing Blockage b) Buffer Blockage	2	6	U
vii)	What are the deciding factors in determining whether to implement a task using software or hardware?	2	1	A
viii)	If a = 1'b1 and b=3'b101 what will be the output of the following Verilog statement {2{a,b}}	2	3	A
Q.2	**Solve any four questions out of six.**	**16**		
i)	Explain SoC Design Flow for configurable processor-based design methodology	4	1	U
ii)	What are the challenges in SoC design that drives parallel architecture	4	2	U
iii)	Write and demonstrate reduction operators in Verilog with examples.	4	3	A
iv)	Write short notes on Rapid Prototyping System.	4	4	U
v)	Write short note on placement.	4	5	U
vi)	Write short note on maze routing.	4	6	U
Q.3	**Solve any two questions out of three.**	**16**		
i)	Explain three stages of evaluation of SoC till platform based SoCs.	8	1	U

	Suggest best possible early choice for following communication requirements. Draw the communication structure. a) Low cost and good flexibility b) Good throughput and Good Flexibility c) Best latency and throughput	8	2	An
iii)	Mention and describe in short, the file formats encountered in the following stages of SoC design a) Requirement gathering b) Model design using HDL c) Synthesis d) Static Timing Analysis (STA) and Signal Integrity Check (SIC) e) Static Timing Analysis (STA) / Dynamic Timing Analysis (DTA) f) Floor plan and placement, global routing, clock tree synthesis g) Power routing h) Tape-out	8	5	U
Q.4	**Solve any two questions out of three.**	**16**		
i)	Design Digital Sound recorder using RTL design technique.	8	3	C
ii)	What is the 'code coverage' verification technique? Enumerate its various types and elaborate on two of them.	8	4	U
iii)	Explain Clock Tree Synthesis in SoC design.	8	6	U

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