K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

July 2024

Program: **B.Tech**
Examination: **LY** (Supplementary)
Course Code: **EXDLC8023**
Date of Exam: 27/07/24

Scheme: **II**
Semester: **VIII**
Course Name: **System On Chip**
Duration: **02.5 Hours**
Max. Marks: **60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		M	CO	BT
Q 1	**Solve any six questions out of eight:**	**12**		
i)	Explain the concepts 'Building a wrong chip'	2	1	U
ii)	What are the impacts of Silicon scaling on system partitioning in SOC design?	2	2	U
iii)	What are the different values a variable can take in Verilog?	2	3	R
iv)	List different types of verification methodologies.	2	4	R
v)	Define the following terms related to physical design of SoC: a) Track b) Row	2	5	U
vi)	Why Clock Tree Synthesis is important in SoC physical design?	2	6	U
vii)	What are the stages of SoC evolution?	2	1	U
viii)	Draw an FSM for edge detector circuit.	2	3	A
Q.2	**Solve any four questions out of six.**	**16**		
i)	Write short note on platform-based design methodology.	4	1	U
ii)	How will you parallelize the following task by using 'Parallelize task phases' technique?	4	2	A

```
int A[],B[],C[];
Task() {
 int i, j;
 for (i=0; i<NBlocks,i++) {
  for (j=0;j<M;j++) B[i][j] = complex_op1(A[i][j]);
  for (j=M-1;j>=0;j--) C[i][j] = complex_op2(B[i][j]);
 }
}
```

iii)	Explain use of the *casex* directives in RTL code with example.	4	3	A
iv)	Explain different techniques used in Analog Mixed Signal Simulation.	4	4	U
v)	What is ECO in SoC physical design?	4	5	U

vi)	Write short note on power routing?	4	6	U
Q.3	**Solve any two questions out of three.**	**16**		
i)	What are the challenges in SoC design? Explain them in brief.	8	1	U
ii)	Explain the selection of processor based on granularity and uniformity of the tasks.	8	2	U
iii)	Draw and explain detailed physical design flow.	8	6	U
Q.4	**Solve any two questions out of three.**	**16**		
i)	Write Verilog code for a sequence detector that can detect non overlapping sequence '1011'.	8	3	A
ii)	Explain bottom-up verification approach with neat diagram.	8	4	U
iii)	Explain floor planning in details.	8	6	U

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