Ref
VI-ETRX
New

T.E/Sem VI / ETRX / Choice based / 10.05-19

(3 Hours) [Total Marks: 80]

(1) Question 1 is compulsory.
(2) Attempt any **three** from the remaining questions.
(3) Draw neat diagrams wherever necessary.

Q1. Answer the following questions: Any 4

a) Justify the need for brown-out detection circuit in embedded systems and the mechanism of implementing the same. (5)

b) What is a Dead Lock State for an embedded system? Give the Types of Deadlock (5)

c) Compare the use of Macros and Functions in terms of Speed and Memory space. (5)

d) What are interrupts and explain the factors that contribute to interrupt response time in a system. (5)

e) Draw the Data Flow Graph for the following

$$y = \frac{\sqrt{a+b}}{c^2}$$ (5)

Q2 (a) Design a Coffee vending machine, for this develop. (20)

- FSM which describes the functioning of the system,
- Requirements /Specifications
- Hardware block diagram
- List of components with justification
- Design challenges and suggest solutions

Q3 (a) What is an inter process communication? Explain the various IPCs mechanisms used in MicroCOS/II. (12)

Q3 (b) Find whether the following Task Set is RMA schedulable (8)

Ti(ei,pi): T1: (1,4) , T2(2,6) T3(3,8)

Compare RMA and EDF Scheduling Algorithms

Q4(a) Compare black box and white box testing. Explain any one On Chip Debugging Technique (10)

Q4 (b) Explain CAN bus Protocol in detail w.r.t features, Applications etc. (10)

Q5 (a) Explain in Detail Design metrics for an embedded system. Which are the tightly constrained metrics , comment (10)

Q5(b) What is a task and various states that a task can lie in for an embedded environment. Explain Context Switching Process. (10)

Q 6. Write a short note on any 2 **(20)**

a) Watch Dog Timer
b) Sensors & Actuators used in Embedded System
c) Priority Ceiling Protocol
d) I2C Communication Protocol.
e) OSTaskCreate( ),OSSemCreate( ),OSFlagPost( ),OSInit( )

TE/ SEM VI / choice based / ETRX/ 16th May 2019

(3 Hours) [Total Marks: 80]

NB: 1) Question No. 1 Compulsory.
2) Attempt any three from the remaining questions.
3) Assume suitable data wherever necessary.

Q.1		Answer **any FOUR**	
	a)	Explain different types of network addresses.	5
	b)	Compare TCP and UDP.	5
	c)	List the categories of UTP cables. How is noise interference minimized in twisted pair cables?	5
	d)	Distinguish between synchronous and statistical TDM.	5
	e)	What is sub netting? List advantages and disadvantages of the same.	5

Q.2.a Explain Different ARQ techniques. Also explain the maximum window size for each with justification. 10

Q.2.b What is piggybacking? Give and example of Piggybacked frame. 10
ketch the appropriate HDLC frames for the following scenario involving Primary station 'A' and two Secondary stations B and C.

1. Primary station A wishes to establish a Normal Response mode link with Secondary stations B and C.
2. Both the stations B and C , send positive ackowledgements to A.
3. Station A sends a polling command to B and B sends 4 data frames. The third frame is lost during transmission.
4. Assuming Selective repeat ARQ, station A sends negative acknowledgement to station B.
5. Station B resends the frame and A sends positive acknowledgement.
6. Station A now polls station C and station C responds with ready response. A sends three data frames to C and C sends positive acknowledgement to indicate the receipt of error free data frames.

Q.3.a Differentiate between IPv4 and IPv6. ExplainTunneling. Determine the class and network address for the following IP addresses(Assuming subnetting is not being used and use default mask) 10
1). 84.42.58.11 2). 195.38.14.13 3). 144.62.12.9

Q.3.b What is meant by 'blocking' in circuit switching networks? Bring out the advantages of multi stage space division switching over single stage switching. (1). Sketch the three stage Space Division switch with N=15, group size of n=5, k=2. What is the condition required to make it non blocking? (2). For the same specifications sketch three stage TST switch using TSI modules. 10

Q.4. a Draw OSI reference model and explain function of each layer. Name the layers responsible for (1). end to end reliability (2). link to link reliability. 10

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Q.4. b Define the utilization or efficiency of the line and derive the expression for stop and wait flow control. Calculate the maximum link utilization for the following cases:- 10

1. Stop and wait flow control
2. Sliding window flow control with window sizes of 4 and 7 .

Link specifications:

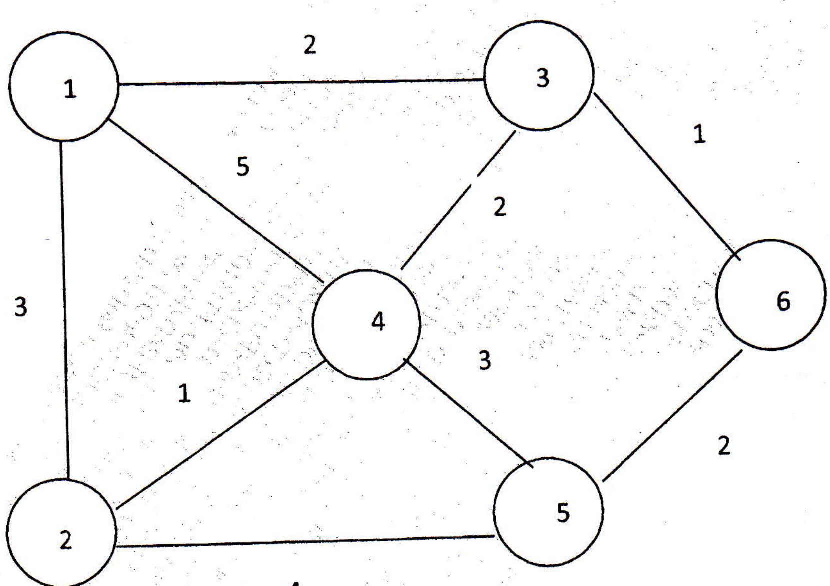
Frame length= 1000 bits/frame

Velocity of propagation = 2 X 10^8 m/sec

Link distance= 20km

Data rate= 20 Mbps

Q.5.a Apply Dijkstra's and Bellman Ford algorithm to the given network and find the least cost path between source node 1 to all other nodes. 10



Q.5.b Draw and Explain TCP header format with the help of a neat diagram. 10

Q.6. Write short note on:(**Any TWO**) 20

a) Congestion control techniques
b) ADSL
c) Compare IPv4 and IPv6
d) CSMA/CD

TE/ETRx - Sem VI / choice based / 22-05-19

(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. 1 is **Compulsory**.
(2) Attempt any **three** questions out of **remaining five**.
(3) Each question carries 20 marks and sub-question carry equal marks.
(4) Assume suitable data if required.

1. Solve **any 4** of the following; (20)
(a) Draw and explain AND gate using pass transistor logic (5)
(b) Implement $Y=\overline{(A+B.C)}$ using dynamic CMOS logic. (5)
(c) Explain low power design consideration (5)
(d) Implement half adder circuit using static CMOS. (5)
(e) Draw schematic for 6T SRAM cell and explain its stability criteria (5)

2. (a) Explain concept of precharge and evolution in dynamic CMOS (10)
(b) Define scaling? Explain various types of scaling in detail (10)

3. (a) Compare Ripple carry adder and carry-look-ahead adder. Explain 4 bit CLA adder implementation. (10)
(b) Explain various techniques of clock generation. Discuss 'H' Tree clock distribution (10)

4. (a) Consider a CMOS inverter circuit with following parameter (10)
$V_{Ton} = 0.6$ V, $V_{Top} = -0.7$V,
$\mu_n Cox = 60\mu A/V^2$, $(W/L)_n = 8$
$\mu_p Cox = 25\mu A/V^2$, $(W/L)_p = 12$

Calculate noise margins and switching threshold of the inverter. The power supply voltage $V_{DD} = 3.3$V
(b) Implement 4:1 MUX using pass transmission logic. Explain advantages of using transmission gates. (10)

5. (a) Explain Barrel shifter in brief. (10)
(b) Draw JK flip flop using CMOS and explain its operation. (10)

6. Write short notes on **any two** of the following: (20)
(a) ESD protection techniques
(b) Interconnect scaling and crosstalk
(c) Sense Amplifier
(d) NAND based ROM array.

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(3 Hrs) Total Marks : 80

NOTE: 1) Question number 1 is compulsory.
2) Attempt any three questions from the remaining five questions.
3) Assume suitable data wherever necessary.

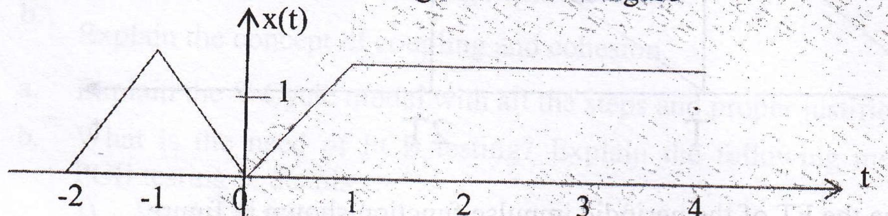
Q.1 a) How will you obtain z-transform of the D.T signal $x(nT)$, from laplace transform of sampled version of $x(t)$, using $z = e^{st}$ **(5)**

b) Check whether the following system is static/dynamic, linear/non-linear, shift variant/shift invariant and casusal/non-causal **(5)**
i) $y(t) = x(t)\cos 100\pi t$
ii) $y(n) = n.x(n)$

c) Determine DTFS for the sequence $x(n) = 4\cos\frac{\pi n}{2}$ **(5)**

d) Prove that energy of a power signal is infinite and power of an energy signal is zero. **(5)**

Q.2 a) Find the even and odd parts of the signal shown in figure **(5)**



b) Verify periodicity of the following continuous time signals, if periodic, find the fundamental period. **(5)**
i) $x(t) = 2\cos(\frac{t}{4})$
ii) $x(n) = 2\cos(\frac{2\pi n}{3}) + 3\cos(\frac{2\pi n}{7})$

c) The analog signal $x(t)$ is given below: **(10)**
$x(t) = 5\cos 50\pi t + 2\sin 200\pi t - 2\cos 100\pi t$
Determine the minimum sampling frequency and the sampled version of analog signal at this frequency. Sketch the waveform and show the sampling points.

Q.3 a) The transfer function of discrete time causal system is given by, **(10)**

$$H(Z) = \frac{1 - Z^{-1}}{1 - 0.2Z^{-1} - 0.15Z^{-2}}$$

Draw cascade and parallel realization.

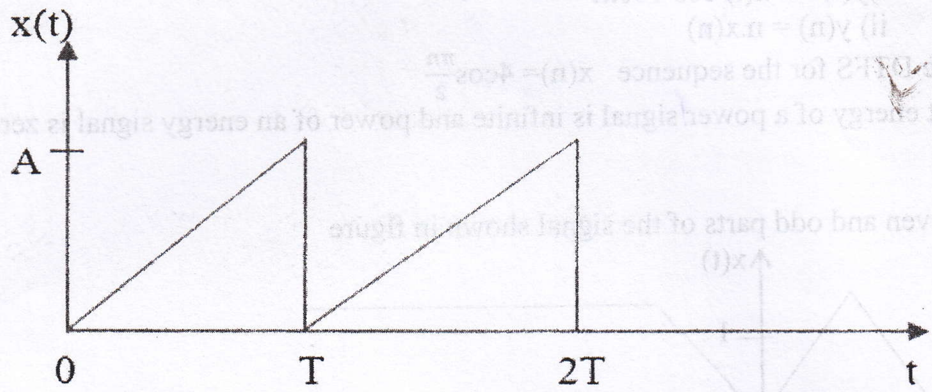
b) Perform the following convolution operation of two functions in time domain. **(10)**
$x_1(t) = e^{-4t}u(t)$ $x_2(t) = u(t-4)$

Q.4 a) Using the Laplace Transform determine the complete response of the system described by the equation : **(10)**

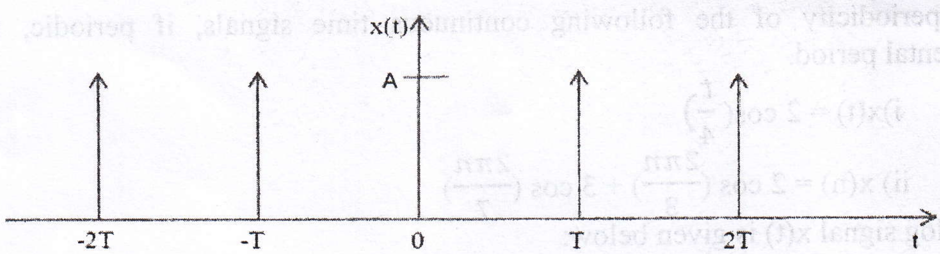
$$\frac{d^2y(t)}{dt^2} + 5\frac{dy(t)}{dt} + 4y(t) = \frac{dx(t)}{dt}$$

Assume that initial conditions of the system are $y(0) = 0$ and $y'(0) = 1$ at input $x(t) = e^{-2t}u(t)$

b) Obtain the exponential form of the Fourier series representation of the signal shown in following signal: **(10)**



Q.5 a) Determine the FT of the periodic impulse function shown in figure. **(10)**



b) A causal LTI system has a transfer function $H(Z) = H_1(Z).\ H_2(Z)$, **(10)**
where $H_1(Z) = \frac{1-0.2Z^{-1}}{1+0.5Z^{-1}}$, $H_2(Z) = \frac{1}{1+0.3Z^{-1}}$
i)If the system is stable, give it's ROC
ii) Find the impulse response of the system
iii) Find the system response if $X(Z) = \frac{1}{1-0.2Z^{-1}}$
iv) Draw the pole-zero diagram.

Q.6 a) Prove Duality property of fourier transform. **(05)**
b) Define the ESD and PSD. What is the relation of ESD and PSD with auto correlation? **(05)**

c) Determine the impulse response for the cascade of two LTI systems having impulse response $h_1(n) = (\frac{1}{3})^n\ u(n)$ and $h_2(n) = (\frac{1}{4})^n\ u(n)$ **(05)**

d) Find initial and final value of signal. **(05)**
$X(S) = \frac{s+1}{s(s+2)}$

88965-M.E

TE (ETRX) Sem VI Choice Based - (DLOC) - 03/06/19

(Time: 3 Hours) **[Total Marks: 80]**

N.B: (1) Question No.1 is compulsory.
(2) Solves any three out of remaining question.
(3) Assume suitable data if necessary.

Q.1		Solve any Four	
	a.	State the phases of new product development.	05
	b.	What are the metrics in software designing?	05
	c.	What is shielding? Explain with neat diagram.	05
	d.	State clearly the limitations and advantages of the Spiral model in EPD.	05
	e.	What is the difference between active and passive component.	05
Q.2	a.	Design the front panel of a function generator by taking care of ergonomics and aesthetic design considerations.	10
	b.	Explain the concept of coupling and cohesion.	10
Q.3	a.	Explain the V Cycle model with all the steps and proper justification.	10
	b.	What is the need of PCB testing? Explain the following methods of PCB testing in details:- i) In-circuit testing ii) Functional testing iii) Boundary scan testing iv) Complex board testing	10
Q.4	a.	What is the role of characterization in case of debugging and troubleshooting?	10
	b.	Explain how mapping of functions to hardware is done in architectural design.	10
Q.5	a.	Write the checklist for developing effective Manuals for the international Market.	10
	b.	How to handle EMI/EMC issues in an Electronic Product?	05
	c.	Explain the need of ESD Protection in PCB Designing.	05
Q.6		Write short note on (any four)	
	a.	Different grounding methodologies	05
	b.	Need of Prototyping	05
	c.	Black box testing and white box testing	05
	d.	Different types of termination methods used in PCB designing	05
	e.	Different software models with advantage and disadvantage	05

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Paper / Subject Code: 88967 / Elective - II Wireless Communication

TE (ETRX) Sem VI Choice Based (DLOC) - 03/06/19

Time: 3 Hrs **Marks: 80**

N.B.
1) Question number ONE is compulsory.
2) Attempt any THREE questions from remaining questions.
3) All questions carry equal marks.

Q1

a) Compare Microcell, Metrocell, Picocell, Femtocell and WiFi in terms of cell radius, power level in watts and number of users. 5

b) Differentiate between CDMA, TDMA and FDMA 5

c) Explain services and features of GSM 5

e) Explain mobility and resource management 5

Q2 a) Consider a cellular system in which the total available voice channels to handle traffic are 480. The area of each cell is 5 sq.km. and the total coverage area of the system is 3000 sq.km. 10

1) For the cluster size of 7, find the no. of channels per cell, no. of clusters, and the system capacity.
2) For the cluster size of 4, repeat the above calculations.
3) Comment on result.

b) Explain different channel assignment strategies in cellular system. 10

Q3 a) What is Huygen's principle of diffraction? Explain Knife –edge Diffraction Model. 10

b) Explain types of Small scale Fading based on multipath time delay spread. 10

Q4 a) Draw a well labelled diagram and explain in detail the architecture of GSM. 10

b) Explain the terms related to GSM 10

1. Diagonal Interleaving 2. Ciphering 3. SIM 4. IMSI Number 5. SMS

Q5 a) Explain IS 95 forward and reverse channels. 10

b) Explain UMTS network architecture in detail with interfaces 10

Q6 Write short notes on following 20

a) Factors influencing Small Scale fading
b) DSSS and FHSS
c) Erlang B and Erlang C system
d) CDMA 2000

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Paper / Subject Code: 88968 / Elective - II Computer Organization and Architecture

E(ETRX) Sem VI Choice Based (DLOC) -03/06/2019

Time: 3 Hours Max Marks: 80

: 1) Question no. 1 is compulsory.
2) Attempt any three out of the remaining five questions
3) Use suitable data, wherever necessary.

Q 1: Attempt any four questions from the following: (20)

a. Explain the function of given CPU registers used in Von Neumann model:
MAR, MDR, IR, PC, SP

b. Differentiate between DRAM and SRAM

c. Why does a superscalar processor use dynamic branch prediction? Justify.

d. Define Micro-operation, Microinstruction, Micro-program, Micro-code.

e. In a multiprocessor system, suppose an application runs on a 4-processor machine and 80% of the application is parallelizable, compute the achievable speedup by applying Amdahl's law.

Q2 (a) Show the multiplication process using Booth's algorithm and multiply the following:
Multiplicand = +23
Multiplier = - 6 (10)

Q2 (b) Explain cache memory mapping techniques with an example (10)

Q3(a) Demonstrate the advantages of pipelining and explain various types of pipeline hazards and their solutions. Give examples (10)

Q3(b) Explain in detail hardwired control. Discuss any one method to implement it. (10)

Q 4(a) Explain page replacement algorithm also find out page faults, page hit, hit ratio for the following string using FIFO and LRU method. Consider page frame size = 3.
2 3 8 9 5 3 8 5 3 3 1 2 4 8 5 4 (10)

Q 4(b) Explain in detail, different types of buses and methods of arbitration. (10)

Q 5(a) Explain in detail, characteristics of RISC and CISC (10)

Q 5(b)Explain Flynn's classification for parallel processing systems. (10)

Q 6. Write short notes on (any four) (20)

a. IEEE 754 format
b. PCI bus Architecture
c. NUMA
d. Cluster computing
e. Control sequence for the execution of SUB R1, (R2) instruction.