

Nov – Dec 2024		
(B. Tech) Program: EXTC Scheme III		
Regular/Supplementary Examination: SY Semester: III		
Course Code: EXC 302 and Course Name: Digital Logic Design		
Date of Exam: 18/12/24	Duration: 02.5 Hours	Max. Marks: 60

Instructions:

- (1) All questions are compulsory.
- (2) Draw neat diagrams wherever applicable.
- (3) Assume suitable data, if necessary.

Q. No.	Question	Max. Marks	CO	BT level
Q 1	Solve any two questions out of three: (05 marks each)	10		
a)	Convert decimal $(153.675)_{10}$ to binary and Hexadecimal form.		1	3
b)	Implement logic circuit for Full Adder.		2	3
c)	Compare Sequential Circuits with Combinational Circuits.		4	3
Q 2	Solve any two questions out of three: (05 marks each)	10		
a)	Explain Classification of RAM and ROM Memories.		3	2
b)	What is a PLA? Explain it with example.		5	2
c)	Write VHDL code for Subtractor circuit.		6	3
Q.3	Solve any two questions out of three. (10 marks each)	20		
a)	Convert SR type Flip Flop into D type Flip-Flop.		4	3
b)	Minimize following expression using Quine Mc Clusky method. $F(P, Q, R, S) = \sum m(2, 6, 8, 9, 10, 11, 14, 15)$		2	3
c)	Simplify $Y = \sum m(1, 3, 4, 5, 7, 10, 12)$ using K-Map & Express in SOP and POS form and design logic circuit using NAND		2	3
Q.4	Solve any two questions out of three. (10 marks each)	20		
a)	Design a 4-bit shift register using S-R Flip-Flops and explain.		4	3
b)	Implement the logic expression using a 4:1 MUX, $F = \sum m(0, 1, 4, 6, 7)$		2	3
c)	Design a three bit ring counter and explain.		4	3
