K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

~~Nov-Dec 2024~~ Jan/Feb 2025
B. Tech Program: Information Technology Scheme III
Supplementary ~~Regular~~ Examination: SY Semester: III
Course Code: ITC304 and Course Name: Computer Organization and Architecture
Date of Exam: ~~28.11.2024~~ 05-02-25 Duration: 02.5 Hours Max. Marks: 60

Instructions:
(1)All questions are compulsory.
(2)Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

Q. No.	Question	Max. Marks	CO	BT level
Q 1	Solve any **two** questions out of three: (05 marks each)	10		
a)	State the difference between Computer organization and architecture.		CO1	U
b)	Explain Basic Instruction Cycle with Interrupt Processing.		CO2	U
c)	Draw and explain flowchart for Restoring division method.		CO3	U
Q 2	Solve any **two** questions out of three: (05 marks each)	10		
a)	Explain Memory Hierarchy Design and its Characteristics in details.		CO4	U
b)	Describe with the help of a neat diagram I/O Module Structure.		CO5	U
c)	Difference between Microcontroller and Microprocessor.		CO6	U
Q.3	Solve any **two** questions out of three. (10 marks each)	20		
a)	Draw and explain the Architecture of 8086 microprocessor		CO1	U
b)	Explain Flynn's Classification and describe the Six stage Pipelining in processor.		CO2	U
c)	Explain the booths algorithm flowchart and Multiply (7) and (5) using Booth's Algorithm.		CO3	Ap

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Q.4	Solve any **two** questions out of three. (10 marks each)	20		
a)	Explain Direct Memory mapping technique in cache memory detail.		CO4	U
b)	Difference between Programmed and Interrupt Driven I/O data transfer technique and explain DMA.		CO5	U
c)	Draw and explain block diagram of 8051 Microcontroller. Implement embedded C program to perform addition of two 16 bit Number(8051 Microcontroller.		CO6	U,Ap

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