K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)

May 2025

B. Tech Program: **Electronics and Telecommunications** Scheme: **III**
Regular Examination: **LY** Semester: **VIII**
Course Code: **EXCDL8023** Course Name: **System On Chip**
Date of Exam: **21/05/2025** Duration: **02.5 Hours** Max. Marks: **60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3)Assume suitable data, if necessary.

		Marks	CO	BT
Q 1	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Discuss the concept of 'Building a wrong chip' and 'Building a chip wrong'.		CO1	An
b)	Discuss briefly about the choice of processor architecture in multi-processor SOC based on granularity and uniformity of tasks.		CO2	U
c)	What is clock skew? Why to avoid it?		CO6	U
Q 2	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Write Verilog code for 4:1 Mux with priority logic		CO3	A
b)	Write short note on emulators.		CO4	U
c)	What is placement in SOC design?		CO5	U
Q.3	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Explain the detailed SoC Design Flow for application Specific processor-based design methodology with proper diagram.		CO1	U
b)	Suggest best possible early choice for following communication requirements. Draw the communication structure. a) Low cost and good flexibility b) Good throughput and Good Flexibility c) Best latency and throughput		CO2	U
c)	Explain Clock Tress Synthesis in details.		CO6	U
Q.4	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Write short note on testbench verification.		CO4	U
b)	Write and explain any five RTL guidelines with example.		CO3	U
c)	Write different formats and describe the contents of the files encountered in different stages of SOC design.		CO5	U

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