K. J. Somaiya Institute of Technology, Sion, Mumbai-22
(Autonomous College Affiliated to University of Mumbai)
Nov –Dec 2025

B.Tech Program: **EXTC** Scheme: **III**
Regular Examination,: **TY** Semester: **V**
Course Code : **EXC501** Course Name: **Digital VLSI Design**
Date of Exam:**24th Nov 25** Duration: **2.5 Hours** Max. Marks:**60**

Instructions:
(1) All questions are compulsory.
(2) Draw neat diagrams wherever applicable.
(3) Assume suitable data, if necessary.

		M	CO	BT
Q 1	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Draw a block diagram of a Carry Save Adder (CSA) for adding seven multi-bit numbers.		5	C
b)	Realize a 4:1 multiplexer using Transmission Gates.		3	C
c)	Draw the circuit diagram of a 6T SRAM cell.		4	U
Q 2	Solve any **two** questions out of three: (05 marks each)	**10**		
a)	Write the advantages and limitations of the static CMOS design style.		3	U
b)	Explain the CMOS latch-up problem in a static CMOS inverter.		2	U
c)	Differentiate between constant field scaling and constant voltage scaling.		1	U
Q.3	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Realize Y = $\overline{A + BC}$ using dynamic CMOS design style. Explain the operation in precharge and evaluate cycle for A=0, B=1 and C=1.		3	A
b)	Design NAND based ROM to store 0100, 1100, 0101 and 0011. Draw the stick diagram for the same.		4	C
c)	Explain the fabrication process of an nMOS transistor with a neat diagram.		1	U
Q.4	Solve any **two** questions out of three. (10 marks each)	**20**		
a)	Design a 3-tap FIR filter using the RTL design process. Calculate the total delay if the propagation delay of an adder is 2 ns and that of a multiplexer is 20 ns.		6	C
b)	Realize a Full Adder using static CMOS mirror circuit.		5	C
c)	Realize Y = $\overline{AB + CD}$ using static CMOS design style. If (W/L)n = 10 and (W/L)p = 20, convert the circuit into equivalent CMOS inverter and find the corresponding (W/L) ratios.		2	C

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Seat No.: