

**K. J. Somaiya Institute of Technology, Sion, Mumbai-22**  
(Autonomous College Affiliated to University of Mumbai)

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|-----------------------------------------------------------------------------|----------------------|----------------|
| Nov – Dec 2025                                                              |                      |                |
| B. Tech Program: Information Technology Scheme:III                          |                      |                |
| Regular Examination: SY Semester: III                                       |                      |                |
| Course Code: ITC304 and Course Name: Computer Organization and Architecture |                      |                |
| Date of Exam: 29/11/2025                                                    | Duration: 02.5 Hours | Max. Marks: 60 |

Instructions:

- (1) All questions are compulsory.
- (2) Draw neat diagrams wherever applicable.
- (3) Assume suitable data, if necessary.

| Q. No. | Question                                                                                                                                              | Max. Marks | CO  | BT level |
|--------|-------------------------------------------------------------------------------------------------------------------------------------------------------|------------|-----|----------|
| Q 1    | Solve any <b>two</b> questions out of three: (05 marks each)                                                                                          | 10         |     |          |
| a)     | Explain block diagram of Basic Instruction Cycle with Interrupt Processing.                                                                           |            | CO2 | U        |
| b)     | Convert $(745.36)_8$ to decimal, binary, and hexadecimal.                                                                                             |            | CO3 | A        |
| c)     | Implement an embedded C program to perform addition of two 16 bit numbers.                                                                            |            | CO6 | A        |
| Q 2    | Solve any <b>two</b> questions out of three: (05 marks each)                                                                                          | 10         |     |          |
| a)     | Draw and explain the flowchart for restoring division algorithm.                                                                                      |            | CO3 | U        |
| b)     | Explain Memory Hierarchy Design and its Characteristics in details.                                                                                   |            | CO4 | U        |
| c)     | Differentiate between Microcontroller and Microprocessor.                                                                                             |            | CO6 | U        |
| Q.3    | Solve any <b>two</b> questions out of three. (10 marks each)                                                                                          | 20         |     |          |
| a)     | Draw and explain the Architecture of the 8086 microprocessor.                                                                                         |            | CO1 | U        |
| b)     | Multiply (-2) and (-5) using Booth's Algorithm and draw and explain the flowchart for Booth's algorithm.                                              |            | CO3 | A        |
| c)     | Explain the Direct Memory mapping technique in cache memory in detail.                                                                                |            | CO4 | U        |
| Q.4    | Solve any <b>two</b> questions out of three. (10 marks each)                                                                                          | 20         |     |          |
| a)     | i) Explain six-stage instruction pipelines. (5M)<br>ii) Explain the difference between Soft wired and Hardwired Control units. (5M)                   |            | CO2 | U        |
| b)     | i) Explain difference between Programmed and DMA I/O data transfer. (5M)<br>ii) Explain the concept of the Direct memory access technique (DMA). (5M) |            | CO5 | U        |
| c)     | Draw and explain the block diagram of the 8051 Microcontroller in details with all registers.                                                         |            | CO6 | U        |